CompactPCI®

ZT 5520

6U CompactPCI Board with Pentium® Pro

Hardware User Manual

ZIATECH CORPORATION

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WHAT'S IN THIS MANUAL

Chapter 1, "**Introduction**," introduces the key features of the ZT 5520. It includes a product definition, a list of product features, a functional block diagram, and a brief description of each block. This chapter is most useful to those who wish to compare the features of the ZT 5520 against the needs of a specific application.

Chapter 2, "**Getting Started**," summarizes the information needed to install and configure your ZT 5520.

Chapter 3, "**CompactPCI Interface**," presents a detailed description of the ZT 5520 interface to the CompactPCI bus. The topics discussed include compatibility and interrupt structure.

Chapter 4, "**Interrupt Controllers**," describes the two Intel-compatible 8259 cascaded interrupt controller sub-systems: a standard ISA-compatible interrupt controller sub-system used for single-processor configuration, and an Advanced Programmable Interrupt Controller (APIC) sub-system used for dual-processor configuration. This chapter summarizes the interrupt sources and the interrupt controllers' programmable registers addressing.

Chapter 5, "**Counter/Timers**," discusses the three programmable counter/timers. It includes a diagram of the counter/timer architecture, a summary of the operating modes and the programmable registers.

Chapter 6, "**DMA Controller**," provides an overview of ZT 5520 DMA architecture and DMA controller operation. The DMA controller programmable registers are also briefly described.

Chapter 7, "**Real-Time Clock**," lists the major features of the real-time clock. The real-time clock programmable registers are also briefly described.

Chapter 8, "**Serial Controller**," discusses operation of the two serial ports and briefly describes the prorammamble registers.

Chapter 9, "**IEEE-1284 Parallel Port Interface**," contains descriptions of the programmable registers for the IEEE-1284 compatible printer interface.

Chapter 10, "**Optional Floppy Disk Interface**," covers the mounting and enabling of an optional local floppy disk interface.

Chapter 11, "**System Registers**," provides register descriptions and a brief overview of the System registers used to control and monitor a variety of functions on the ZT 5520.

Chapter 12, "**Watchdog Timer**," explains operation of the watchdog timer and includes code for arming and strobing the timer.

Chapter 13, "**Parallel I/O**," explains the operation and use of the ZT 5520's digital I/O outputs.

Chapter 14, "**Programmable LED**," provides code for turning the user LEDs on and off.

Chapter 15, "**Thermal Considerations**," addresses the special cooling issues associated with the Pentium Pro processor.

Chapter 16, "**Flash Memory**," discusses on-board flash memory, including the system BIOS EEPROM. Recovery from BIOS EEPROM corruption and BIOS EEPROM modification are covered in this chapter.

Chapter 17, "**Enhanced IDE Interface**," provides an introduction to the ZT 5520's Enhanced IDE interface controller.It covers the ZT 5520's support for remote EIDE disk drives as well as for on-board solid state IDE capability through the optional ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter.

Appendix A, "**Board Configuration**," describes the BIOS setup mechanism, DIP switches, and cuttable traces on the ZT 5520. This appendix details factory default settings as well as information to tailor your board to a specific application.

Appendix B, "**Specifications**," contains the electrical, environmental, and mechanical specifications for the ZT 5520. It also provides illustrations of the board dimensions and connector locations, connector pinout tables, and example schematics showing connection of various peripherals to the rear-panel user I/O connector.

Appendix C, "**Digital I/O ASIC System Setup Considerations**," offers tips for safely connecting the parallel I/O to external devices.

Appendix D, "**PCI Configuration Space Map**," presents the generic layout of the PCI Configuration Header for all PCI compliant devices. It also contains a table showing the PCI bus mapping of the ZT 5520's on-board devices.

Appendix E, "**Customer Support**," offers technical assistance and warranty information and the necessary information should you need to return your ZT 5520 for repair.

1. INTRODUCTION

This chapter provides a brief introduction to the ZT 5520. It includes a product definition, a list of product features, a functional block diagram, and a description of each block. Unpacking information and installation instructions are found in Chapter 2, "Getting Started".

PRODUCT DEFINITION

The ZT 5520 is a high-performance, Single/Dual Pentium® Pro processor-based single board CompactPCI™ computer in the Eurocard 6U form factor. It utilizes the Intel® 440FX chipset to provide extremely high PCI performance and the latest in memory and I/O technology. The board meets the needs of a wide range of industrial control and processing applications.

FEATURES

- Compliant with the CompactPCI Specification, PICMG 2.0, Version 2.1
- Single/Dual 200 MHz Pentium Pro processor operation
- Jumperless setup
- Built-in numeric co-processor support (Pentium Pro processor)
- 16 Kbytes of CPU L1 cache (per Pentium Pro processor)
- 256 or 512 Kbytes of CPU L2 Cache (per Pentium Pro processor)
- PCI mezzanine interface (Primary PCI bus)
- Drives two CompactPCI Buses (up to 14 slots)
- 64, 96, or 128 Mbytes of DRAM (Can support up to 512 Mbytes in the future)
- 2 Mbytes of flash memory (expandable to 4 or 8 Mbytes)
- Standard AT® peripherals include:
  - – Three counter/timers (one 8254)
  - – Real-time clock/CMOS RAM (146818)
  - – Two enhanced DMA controllers (8237)
  - – 8042 compatible keyboard controller
- Advanced Programmable Interrupt Controller (I/O APIC)
- Enhanced IDE controller
- CompactFlash-to-IDE Mezzanine Adapter capability (ZT 96061 – optional)
- Floppy disk controller

- IEEE® 1284 printer port (ECP/EPP compatible)
- Two 16C550 RS-232 serial ports
- USB (Universal Serial Bus)
- Single stage watchdog timer
- Speaker interface
- Two on-board high efficiency CPU programmable DC-DC converters
- On-board high efficiency 3.3 V DC-DC converter
- Push-button reset
- Push-button NMI
- Software programmable LEDs
- DC power monitors (3.3 V and 5 V)
- Compatible with the following software: MS-DOS®, OS/2®, UNIX®, QNX®, VRTX32®, VxWorks®, Windows® 3.1 and 3.11, Windows 95, and Windows NT®
- Burned-in at 50° Celsius and tested to guarantee reliability
- Five-year warranty

RELIABILITY

Reliability information for the ZT 5520 is as follows:

- MTBF: 5.5 Years
- MTTR: 5 Minutes (based on board replacement)

DEVELOPMENT CONSIDERATIONS

Ziatech offers a DOS software development system for ZT 5520 applications. Ziatech DOS is Microsoft's MS-DOS residing on the ZT 5520. The DOS system provides a development platform similar to a PC, enabling applications to be developed quickly. DOS includes support for many of the ZT 5520 peripherals and is supported by a large number of development tools such as program editors, compilers, assemblers, and debuggers. Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for configuration and operating instructions.

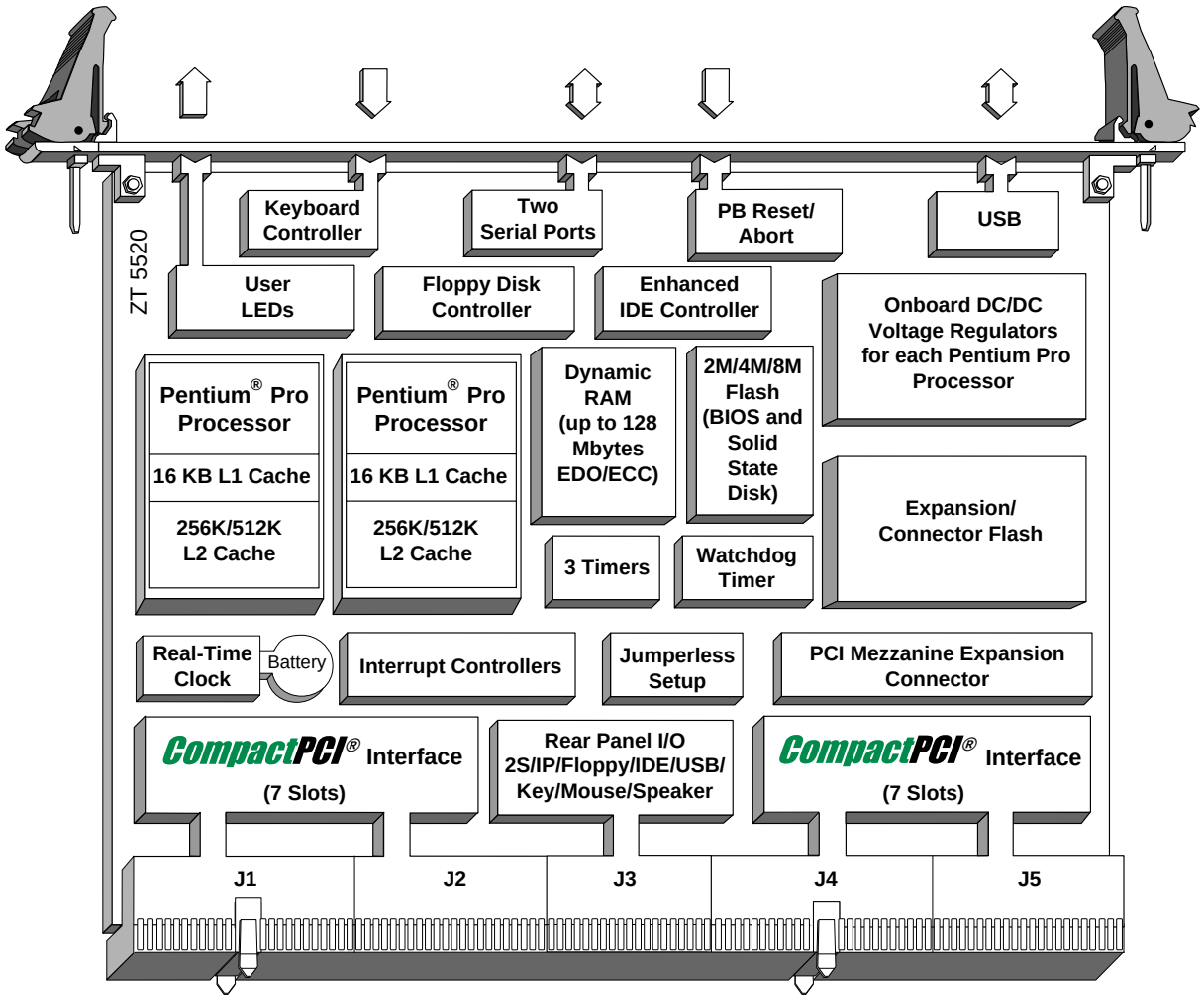
Ziatech also offers software development kits for QNX®, VxWorks®, and Windows NT™ operating systems. Contact Ziatech for details.

FUNCTIONAL BLOCKS

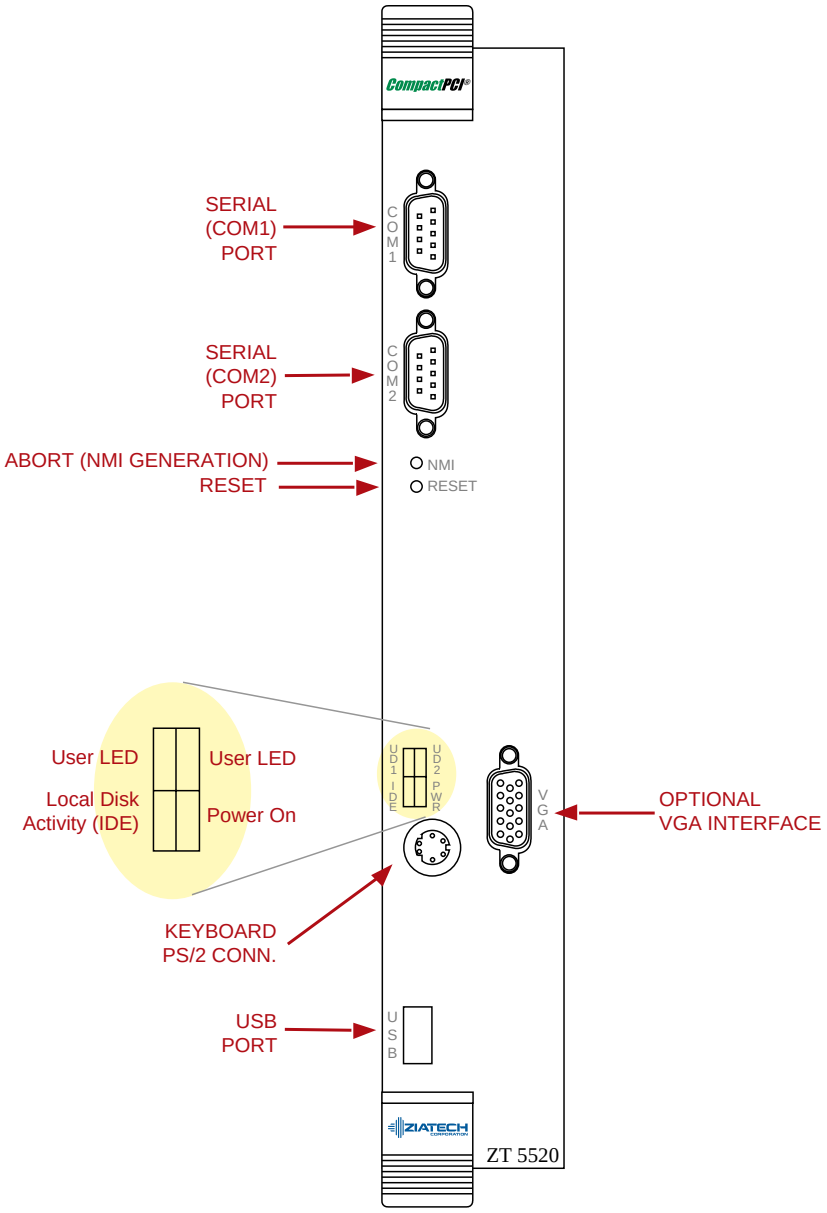
Below is a functional block diagram of the ZT 5520. The blocks correspond to topics remaining in this chapter.

The following topics, not represented on the diagram, are also included in this chapter:

- Speaker Interface
- DMA
- Intel 440FX PCI Interface
- Chipset
- Mouse
- IEEE-1284 Parallel Port/Printer Interface



Functional Block Diagram



Front Panel

CompactPCI Bus Interface

The ZT 5520 operates in a 6U CompactPCI system. The CompactPCI standard is electrically identical to the PCI local bus standard but has been enhanced to support rugged industrial environments and more slots. The ZT 5520 uses dual DIGITAL Semiconductor™ 21153 PCI-to-PCI bridges to support both the J1/J2 bus and the J4/J5 bus with CompactPCI. This allows the ZT 5520 to support up to 14 CompactPCI peripherals (all bus masters) without the need for an external bridge board.

Refer to the *DIGITAL Semiconductor PCI-to-PCI Bridge Data Sheet* for more information on the 21153 bridge chip. The data sheet is in Adobe Acrobat format (PDF) and is available online at:

http://developer.intel.com/design/bridge/applnots/27806902.pdf

See Chapter 3, "CompactPCI Interface," for an overview of the ZT 5520 interface to the CompactPCI bus architecture.

Pentium Pro Processors

The ZT 5520 supports the Pentium® Pro processor family, commonly referred to as the P6. The ZT 5520 operates the external microprocessor bus at either 60 or 66 MHz. The P6 operates internally at 2x, 2.5x, 3x, 3.5x, or 4x the microprocessor bus speed.

The PCI bus always operates at 1/2 the external microprocessor bus speed. Not all processor speeds are offered by Ziatech. Contact Ziatech for latest product offerings or refer to the web site at http://www.ziatech.com.

Each Pentium Pro processor includes 16 Kbytes of cache (referred to as L1 cache). This L1 cache is configured as 8 Kbytes of code and 8 Kbytes of data cache, and supports both write-through and write-back cacheing. Additionally, each Pentium Pro processor contains a secondary 256 Kbyte or 512 Kbyte L2 cache to further enhance memory performance.

Intel 440FX PCI Interface ChipSet

The 440FX chipset from Intel is designed to maximize throughput on the PCI bus. It is a third generation PCI chipset capable of burst mode transfers to 110 Mbytes per second. The 440FX chipset sets the standard for the Pentium Pro processor-class of computers.

Refer to Appendix D, "PCI Configuration Space Map," for more information about Intel's 440FX chipset.

On-Board Voltage Conversion

The ZT 5520 contains four DC/DC converters. Each Pentium Pro processor is supported by a converter that is self-configured for the processor's required core voltage. Another converter is used for the processor's L2 cache and other 3.3 V devices such as DRAM and the chipset. The final converter is used to drive the CPU (GTL+) bus. The board is configured from the factory to the correct voltage for the loaded processor(s).

Jumperless Setup

There are no jumpers on the ZT 5520. Configuration options on the ZT 5520 are selectable through the "BIOS SETUP Utility Screen." See the section "Setup" in Chapter 2 for more information about system configuration.

PCI Mezzanine

A PCI bus (Primary, Bus 0) mezzanine connector (J18) is located on the ZT 5520 which can be used to support PCI mezzanine boards such as Ziatech's zPM11 SVGA Mezzanine Board (ordering option V1 or V2).

Expansion Connector

An expansion connector (J17) is located on the ZT 5520 to allow for optional on-board solid state IDE through the ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter (ordering option M0-M3). The ZT 96061 is designed to accommodate CompactFlash expansion cards. These cards appear to the system as a hard drive and are automatically supported by most operating systems.

See the section "Solid State IDE Option" in Chapter 17, "Enhanced IDE Interface," for more information on the CompactFlash option.

Memory and I/O Addressing

Custom 200-pin DRAM modules are used on the ZT 5520 for local memory (J19). Up to four 32 Mbyte DRAM memory modules may be stacked on the ZT 5520, for a total of up to 128 Mbytes of DRAM, 64 Mbytes minimum. Additional DRAM may be installed on the ZT 5520 after the system has been purchased, however all memory upgrades must be installed at the factory. Contact Ziatech for more information.

The DRAM is implemented as Error Correcting Coded (ECC), which will correct single bit errors (97% of all DRAM errors are single bit errors) and report multiple bit errors to the operating system. The standard option for the ZT 5520 is to use ECC memory; however, the design does support non-ECC operation.

In addition to DRAM, the ZT 5520 can support on-board up to 8 Mbytes of flash memory (2 Mbytes is standard). The flash memory contains the system BIOS, with the remainder allocated as solid-state disk.

All memory and I/O addresses are forwarded to the PCI bus; thus, any device on the PCI bus has access to the full memory and I/O address range. Any I/O or memory addresses that are not actively decoded are taken (subtractively decoded) by the ISA bridge (PIIX3 device).

Serial I/O

The ZT 5520 provides two 16C550 PC-compatible serial ports. The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through the front panel as COM1 (J13) and COM2 (J12). For more information on ZT 5520's serial ports, see Chapter 8, "Serial Controller."

Interrupts

Two enhanced 8259 style interrupt controllers and an I/O Advanced Programmable Interrupt Controller (I/O APIC) provide a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Fixed and rotating priorities
- Individual input masking
- Individual input routing

Interrupt sources include:

- Counter/timers
- Serial I/O
- Real-time clock
- Keyboard
- Printer
- Floppy disk
- IDE interface
- Digital I/O
- CompactPCI backplane (four interrupts)

Enhanced capabilities include the ability to configure each interrupt level for active high going edge or active low level inputs. See Chapter 4, "Interrupt Controllers," for more information on the ZT 5520's interrupt controllers.

Counter/Timers

Three 8254 style counter/timers are included on the ZT 5520 as defined for the PC/AT. Operating modes supported by the counter/timers include interrupt on count, frequency

divider, square wave generator, software triggered, hardware triggered, and one shot. See Chapter 5, "Counter/Timers," for more information.

DMA

Two enhanced 8237 style DMA controllers are provided on the ZT 5520 for use by the on-board peripherals. DMA channel 2 is assigned to the optional floppy drive (J22) and DMA channels 0 or 3 are assigned to the parallel printer port (J3). For advanced mode support, see Chapter 9, "IEEE-1284 Parallel Port Interface."

See Chapter 6, "DMA Controller," for more information about the DMA controller.

RESET

The ZT 5520 is automatically reset with a precision voltage monitoring circuit that detects when Vcc is below the acceptable operating limit of 4.75 V. In addition, the on-board 3.3 V power supply is monitored and resets the ZT 5520 when below 3.0 V. The system will also reset if either Pentuim Pro processor core voltage varies by more than 7% of its programmed value. Other sources of reset include the watchdog timer, local push-button switch (SW2 on the ZT 5520's front panel), and the CompactPCI Bus reset signal, PRST# (CT3 and CT44 must be installed).

The ZT 5520 responds to any of these reset sources by initializing local peripherals and driving the local CompactPCI bus resets.

Watchdog Timer

The watchdog timer optionally monitors system operation. Failure to strobe the watchdog timer within a set time period results in a system reset. Chapter 12, "Watchdog Timer," explains operation of the watchdog timer and includes code for arming and strobing the timer.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS SETUP information (see the section "Setup" in Chapter 2).

Chapter 7, "Real-Time Clock," lists the major features of the real-time clock and provides register descriptions.

IEEE 1284 Parallel Port/Printer Interface

The ZT 5520 includes an IEEE® 1284 compatible parallel port accessible via the rear-panel user I/O connector (J3). This parallel port/printer interface enables connection to a

printer or other parallel port devices such as software keys required by many application packages. The parallel port is ECP/EPP compatible. The mode (Normal, Extended, EPP, ECP) for the printer interface is selectable through the BIOS SETUP mechanism (see the section "Setup" in Chapter 2).

Chapter 9, "IEEE 1284 Parallel Port Interface," contains descriptions of the programmable registers for the IEEE-1284 compatible printer interface.

Universal Serial Bus (USB)

The emerging Universal Serial Bus (USB) will provide a common interface to slower speed peripherals in the future. Functions such as keyboard, serial ports, printer port, and mouse ports will be consolidated into USB, greatly simplifying the cabling requirements of future computers. The ZT 5520 provides one USB port through the front panel connector (J6) and one USB port through the rear-panel user I/O connector (J3) for this capability.

Speaker Interface

For external speaker interfacing, the ZT 5520 supports an external AT-compatible speaker through an on-board 2-pin header (SPK1), located next to connector (J6).

Floppy Interface

The floppy interface supports a floppy disk through the rear-panel user I/O connector (J3). This connector provides a mechanism for the floppy drive to be remotely mounted (via a rear-panel transition board), or accessed on the ZT 5980B System Utility Board. The ZT 5980 provides a 3.5" slimline floppy drive and optional hard drive for development system or target applications.

Enhanced IDE Interface

The ZT 5520's EIDE interface provides two EIDE channels for interfacing with up to four drives. The EIDE interface is incorporated into the Intel PIIX3 (82371SB), thus it utilizes the Peripheral Component Interconnect (PCI) bus to give exceptional EIDE performance. The EIDE interface can sustain a maximum transfer rate of 22 Mbytes per second between the EIDE drive buffer and PCI.

See Chapter 17, "Enhanced IDE Interface," for more information.

Keyboard Controller

The ZT 5520 includes an on-board PC/AT® keyboard controller, available through the front panel connector (J9).

Mouse

A PS/2 style mouse controller is provided by the ZT 5520. The system BIOS supports standard PS/2 bus mouse devices through the rear-panel user I/O connector (J3). Use of the PS/2 mouse controller leaves both serial ports available for other communication.

LED Indicators

LEDs are provided on the front panel for the following features:

- Local IDE activity
- Power on
- User Definable 1
- User Definable 2

Chapter 14, "Programmable LED," provides code showing how to change the status of the LEDs.

2.GETTING STARTED

This chapter summarizes the information needed to make the ZT 5520 operational. Read this chapter before attempting to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Do not return any product to Ziatech without a Return Material Authorization (RMA) number. The "Returning for Service" section in Appendix E explains the procedure for obtaining an RMA number from Ziatech.

WHAT'S IN THE BOX

The items listed below are included with a ZT 5520 order. System level products, such as the DOS development package, include additional items not shown. If a system level product has been ordered, refer to the system manual for the packing list.

- ZT 5520 6U CompactPCI CPU Board with Single/Dual Pentium Pro Processors in anti-static bag (save the anti-static bag for storing or returning the ZT 5520)
- Optional PCI peripherals
- Optional cables

Warning: Like all equipment utilizing MOS devices, the ZT 5520 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 5520 to handle the board.

SYSTEM REQUIREMENTS

The ZT 5520 is designed for use with or without a CompactPCI bus backplane. The ZT 5520 is electrically, mechanically, and functionally compatible with the *CompactPCI Specification, PICMG 2.0, Version 2.1*.

Ziatech recommends vertical mounting. The ZT 5520 is supplied with an integrated processor fan/heatsink to allow operation between 0º and approximately 55º C ambient. Refer to the section, "Absolute Maximum Ratings," in Appendix B for specific temperature specifications for the different processor options.

MEMORY CONFIGURATION

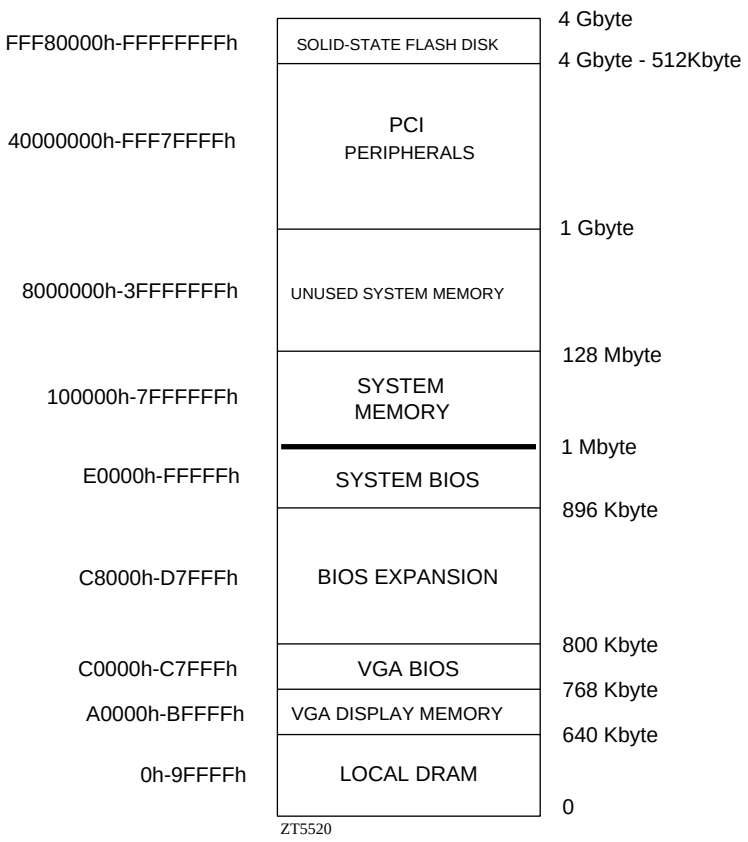
The ZT 5520 addresses up to 4 Gbytes of memory. The address space is divided between memory local to the board and memory located on one of the two CompactPCI buses. Any memory not reserved or occupied by a local memory device (DRAM/flash) is available to the CompactPCI bus.

The ZT 5520 is populated with several memory devices. Local DRAM is contained in a unique stackable memory architecture (through connector J19) that supports up to four 32 Mbyte DRAM memory modules, for a total of up to 128 Mbytes of DRAM, 64 Mbytes minimum. Additional DRAM may be installed on the ZT 5520 after the system has been purchased, however all memory upgrades must be installed at the factory. Contact Ziatech for more information.

Local flash memory is soldered directly to the board. There is space for two flash devices, which may be either 2 Mbyte or a 4 Mbyte devices, for a total of up to 8 Mbytes of flash memory. The 2 Mbyte devices do not require +12 V operation. The 4 Mbyte devices do require +12 V +/- 5% for programming operations.

Additional flash capability is supported via the onboard flash/IDE expansion connector (J17). This option implements the ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter which is designed to accommodate CompactFlash expansion cards. These cards appear to the system as a hard drive and are automatically supported by most operating systems. See the section "Solid State IDE Option" in Chapter 17, "Enhanced IDE Interface," for more information on the CompactFlash option.

The "Memory Address Map" illustration shows default memory addressing for the ZT 5520.

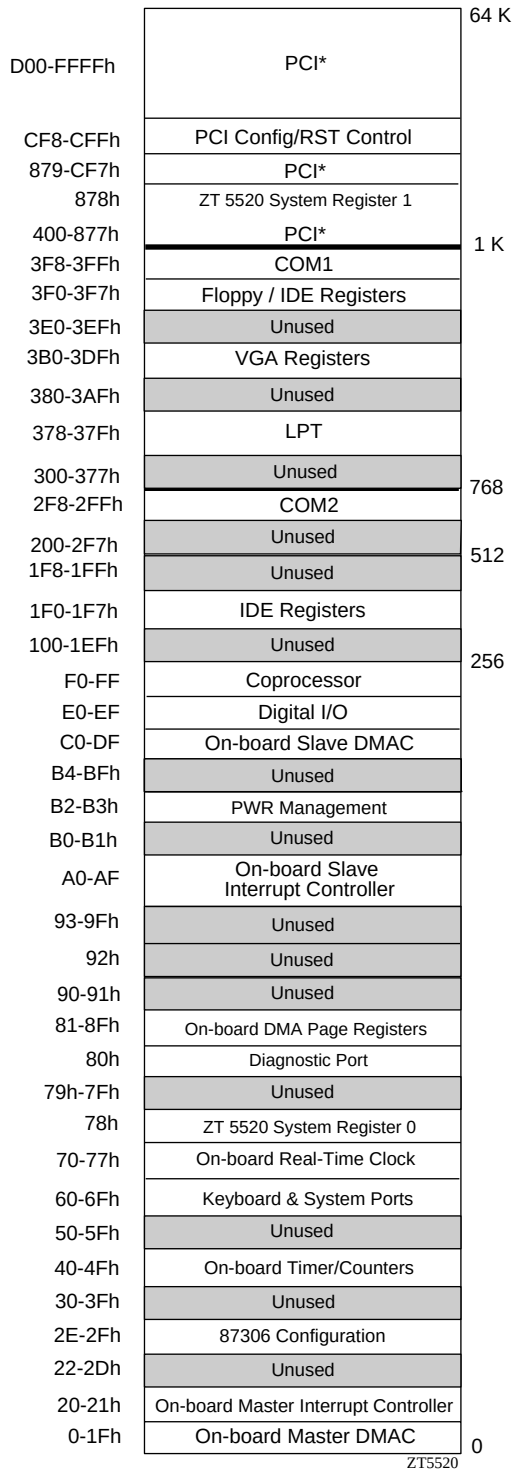


Memory Address Map

I/O CONFIGURATION

The ZT 5520 addresses up to 64 Kbytes of I/O using a 16-bit I/O address. The address space is divided between I/O local to the board and I/O on the CompactPCI bus. Any I/O space not occupied by a local I/O device is available for the CompactPCI bus.

The ZT 5520 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in the "I/O Address Map" illustration.



*ISA Peripherals decode 10 bits of address. Therefore they will alias throughout the 16 bit I/O space at ranges: x100-x3FFh, x500-x7FFh, x900-xBFFh, xD00-xFFFh.

I/O Address Map

CONNECTOR CONFIGURATION

As shown in the "Connector Locations" drawing, the ZT 5520 includes several connectors to interface to application-specific devices. Refer to the "Connectors" section in Appendix B for complete connector descriptions and connector pinouts.

SWITCH AND CUTTABLE TRACE DESCRIPTIONS

The ZT 5520 includes several switch and cuttable trace configuration options for features that cannot be provided through the software SETUP mechanism (discussed in the "Setup" section below). Refer to Appendix A, "Board Configuration," for details.

USING OPTIONAL COMPACTFLASH SOLID STATE IDE

Chapter 17, "Enhanced IDE Interface," includes information on how the ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter works with the ZT 5520's enhanced IDE controller. It provides information on disk drive configuration and support, input characteristics, as well as how to install and remove the ZT 96061 and CompactFlash cards. Read Chapter 17 before attempting to use the ZT 96061.

REMOVING THE ZPM MEZZANINE CARD

Ziatech zPM mezzanine cards plug into the 150-pin PCI mezzanine connector provided on many Ziatech CPUs (J18 on the ZT 5520). Mechanical connection of the boards is reinforced by metal or nylon stand-offs screwed through mounting holes in each board.

Note: If it is necessary to disconnect a zPM mezzanine card, Ziatech recommends removing only the screws attaching the card to the stand-offs. If it is necessary to remove the stand-offs from the CPU, be aware that on some CPUs washers may be located between the PCB and the stand-offs. Be sure to retain and re-install these washers to their original position if they are removed for any reason.

Care should also be taken when installing and removing the zPM mezzanine card to prevent premature wear or accidental bending of the 150-pin (and on some mezzanine cards, an additional 16-pin) connector. When removing the card, disengage the pins evenly across the length of the connectors instead of prying only from one side. It may be helpful to gently wiggle the card from side-to-side when removing it.

Warning: To avoid damage to the CPU and the mezzanine card, perform the installation and removal at a static-free workstation.

SETUP

The following topics present a brief introduction to the setup and configuration of the ZT 5520. For documentation specific to the BIOS and other utilities, see the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual (shipped with Ziatech Development Systems).

System Configuration Overview

The Ziatech Industrial BIOS and MS-DOS operating system software is preprogrammed in the ZT 5520's on-board flash memory. The BIOS includes embedded support to allow the ZT 5520 flash memory to be used as a solid-state drive (SSD) in the MS-DOS environment. Ziatech also supplies SSD support for other popular operating systems such as Windows NT and QNX (contact Ziatech for SSD drivers for specific operating systems).

The ZT 5520 is configured during the boot sequence by the BIOS. The BIOS uses system configuration information stored as SETUP parameters.

To access the SETUP utility, either boot the system and press the **"S"** key during the system RAM check, or run the SETUP.COM utility from the MS-DOS prompt.

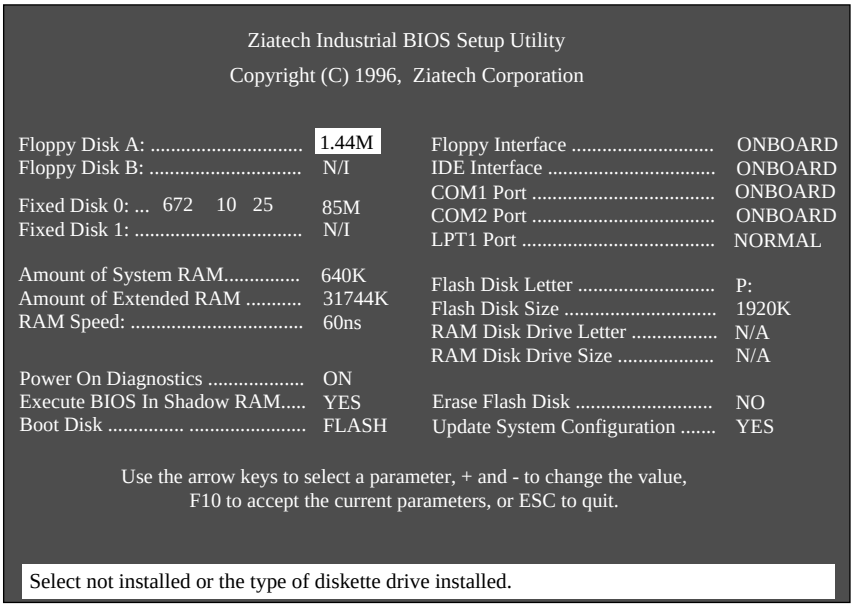
The SETUP parameters are saved in the battery-backed RAM portion of the ZT 5520's real-time clock device. The SETUP parameters can also be saved in a file format, or as the programmed BIOS defaults.

When SETUP is run, an interactive configuration screen is displayed, as shown in the "BIOS SETUP Utility Screen Example" illustration.

Note: the SETUP program is a generic utility used for all Ziatech processor boards. Some parameters not applicable to the ZT 5520 may be labeled "N/A".

The BIOS SETUP screen is organized as a single screen. The SETUP screen allows the user to select options for such items as base memory and extended memory size selection, boot source, hard disk type, and floppy disk type.

The parameters in the SETUP screen are easily changed. Use the arrow keys to select a parameter, then press **+** or **-** to step through the valid choices for that parameter. A dynamic help line at the bottom of the screen helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter invalidates another parameter, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them.



ZT5520

BIOS SETUP Utility Screen Example

Operating System Installation

It is usually necessary to install an operating system such as Windows NT or QNX on the ZT 5520 system. This section describes the generic OS installation process. For OS-specific information, refer to the documentation provided by the OS vendor.

Note: If your ZT 5520 implements the ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter option, please note that you may have difficulty installing the QNX operating system, ver. 4.24, on CompactFlash cards. If problems occur, restart the install program and specify regular IDE drivers (Fsys.ide) instead of the default EIDE drivers (Fsys.eide). See Chapter 17, "Enhanced IDE Interface," for more information on the CompactFlash option.

1. Use the SETUP utility (shown in the "BIOS SETUP Utility Screen Example" illustration) to configure the appropriate peripheral devices. Note that the Fixed Disk parameters (used for EIDE drives) include an "AUTO" setting which will cause SETUP to query the drive to determine the correct geometry (cylinders/heads/sectors).

2. Select the proper boot source in the SETUP utility depending on the OS installation media that will be used. For example, if the OS includes a bootable installation floppy, select "FLOPPY" for "Boot Disk" and reboot the system with the installation floppy installed in the floppy drive.

3. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. See the "On-Board Device PCI Bus Mapping" table in Appendix D for a list of the PCI devices used on the ZT 5520.

4. When installation is complete, the system should be rebooted and the SETUP "Boot Disk" parameter should be set for the appropriate boot media.

3. COMPACTPCI INTERFACE

The ZT 5520 operates with the CompactPCI bus architecture to support additional I/O and memory mapped devices as required by the application. This chapter gives a brief overview of the CompactPCI architecture and its effect on the operation of the ZT 5520.

For more detailed information on CompactPCI, obtain the complete specification from PICMG (PCI Industrial Computers Manufacturers Group) for a nominal fee. Contact PICMG via their web site at http://www.picmg.org. A short form specification is also available on Ziatech's web site at http://www.ziatech.com.

COMPACTPCI OVERVIEW

CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification*. It has been optimized for industrial and/or embedded applications that require a more robust mechanical form factor than Desktop PCI. CompactPCI uses industry standard mechanical components and high performance connector technologies to provide a system well suited for rugged applications. CompactPCI provides a system that is electrically compatible with the PCI Specification, allowing low cost PCI components to be used. CompactPCI is an open standard supported by the PICMG (PCI Industrial Computers Manufacturers Group), which is a consortium of companies involved in utilizing PCI for embedded applications.

INTENDED APPLICATIONS

CompactPCI appeals to customers that require the following capabilities:

- PCI performance
- 32- and 64-bit data transfers
- 8 PCI slots per system
- Industry standard software support
- 3U small form factor (100 mm by 160 mm)
- 6U form factor (233 mm by 160 mm)
- Eurocard packaging
- Wide variety of available I/O

APPLICABLE DOCUMENTS

For more information on the *PCI Local Bus Specification,* refer to the following list of publications.

- *PCI Local Bus Specification*, PCI Special Interest Group, 5200 N. E. Elam Young Parkway, Hillsboro, Oregon, USA, 9724-6497, (503) 696-2000
- IEC 297-3, *Eurocard Specification*, Bureau Central de la Commission Electrotechnique Internationale, 1 rue de Varembe, Geneva, Switzerland, 011.412.291.90228
- IEC-1076-4-101, *Draft Specification for 2 mm Connector Systems*, International Electrotechnical Commission, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY, USA 10036
- IEEE1101.1-1991, *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors*, Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331
- IEEEP1101.10-3.X, *IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE1101.1 Equipment Practice,* Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331
- ANSI/VITA 1-1994, *VME64 Specification,* VITA, 10229 N. Scottsdale Rd., Suite B, Scottsdale, AZ, USA, 85253

4. INTERRUPT CONTROLLERS

The ZT 5520 includes two interrupt controller sub-systems: a standard ISA-compatible interrupt controller sub-system used for single-processor configuration, and an Advanced Programmable Interrupt Controller (APIC) sub-system used for dual-processor configuration. The BIOS automatically detects the number of processors on the board and enables the appropriate sub-system.

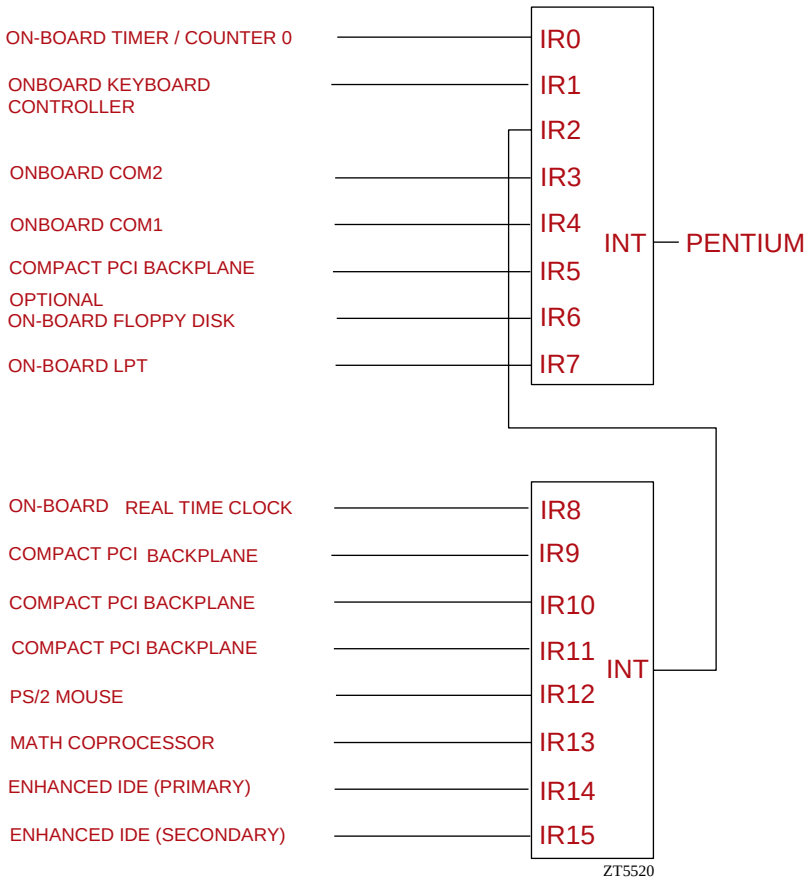
SINGLE-PROCESSOR CONFIGURATION

A ZT 5520 implementing a single processor uses the ISA-compatible interrupt controller sub-system. This sub-system consists of two Intel-compatible 8259 cascaded interrupt controllers incorporated into the Intel PIIX3 (82371SB) chipset that provide a programmable interface between interrupt-generating peripherals and a single CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device.

The major features of the interrupt architecture are listed below.

- 15 individually maskable interrupts
- Jumperless configuration
- Level-triggered or edge-triggered recognition
- Fixed or rotating priorities
- PCI Interrupt support
- PCI Extended Mode register support

The interrupt architecture is illustrated in the "Programmable Interrupt Controller Architecture" figure. The ZT 5520 supports the Extended Mode Register, which allows individual programming of low-level triggered or active high-edge triggered interrupts.



Progammable Interrupt Controller Architecture

INTERRUPT SOURCES

The interrupt sources are summarized below.

PCI Interrupts

The CompactPCI bus interrupts have been assigned to IRQ9, IRQ10, IRQ11, and IRQ5 on the ZT 5520 Programmable Interrupt Controller (PIC). These interrupts are automatically configured by the BIOS. The CompactPCI bus defines these four interrupts as INTA, INTB, INTC and INTD, respectively. These interrupts are all active low, level-triggered interrupts.

On-Board Interrupts

On-board interrupt sources include the keyboard controller, serial ports (COM1, COM2), parallel printer port, real-time clock, timer/counters, math coprocessor, IDE controller and floppy disk.

PROGRAMMABLE REGISTERS

Each interrupt controller includes four initialization registers, three control registers, and three status registers. The I/O port addressing for the interrupt controllers is given in the "Interrupt Controller Register Addressing" table below. The base address of the master interrupt controller is 20h and the base address of the slave interrupt controller is A0h.

Interrupt Controller Register Addressing

Address	Register	Operation
Base+0h	IRR, ISR, IPR	Read
Base+0h	ICW1	Write
Base+0h	OCW2, OCW3	Write
Base+1h	OCW1	Read/Write
Base+1h	ICW2, ICW3, ICW4	Write

DUAL-PROCESSOR CONFIGURATION

A ZT 5520 implementing dual processors uses the Advanced Programmable Interrupt Controller (APIC) sub-system. This sub-system consists of one Intel 82093AA I/O APIC (IOAPIC) and two CPU local APICs (one inside each processor). The local APICs and the IOAPIC communicate over a dedicated bi-directional APIC bus. The figure below "APIC Sub-System Functional Block Diagram" shows an overview of the symmetric I/O APIC mode of operation.

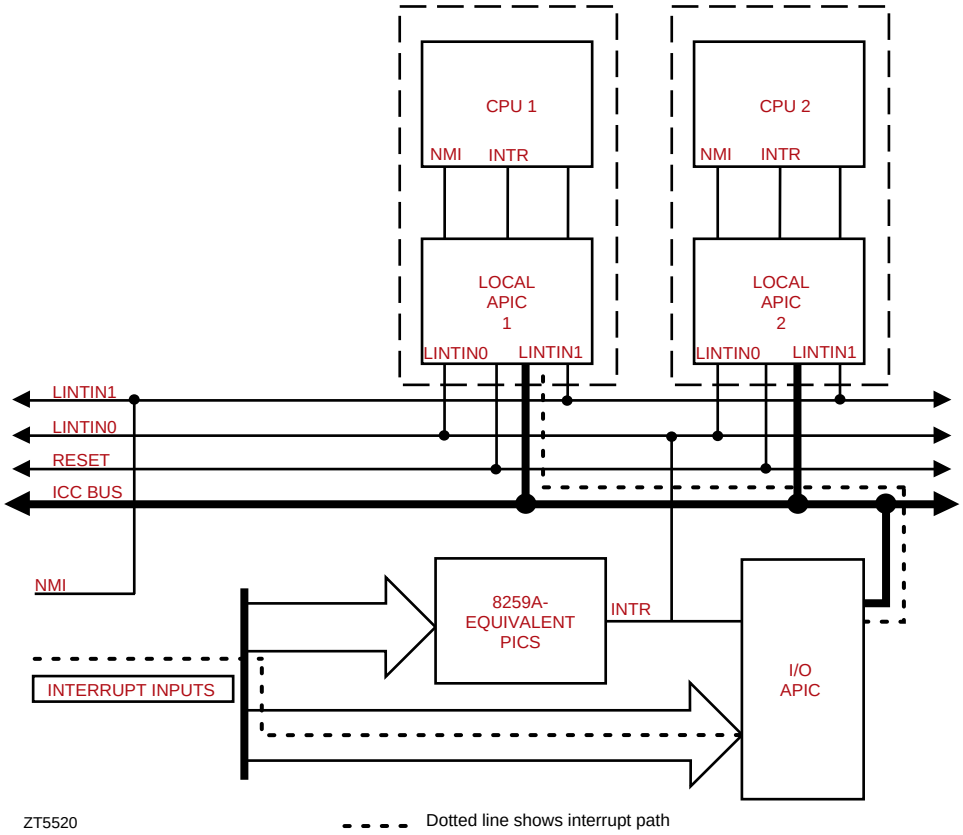
The CPU's local APIC unit controls the acceptance of interrupts broadcast on the APIC bus. The local unit also provides interrupt pending, nesting, and masking, as well as inter-processor interrupt routing.

The IOAPIC unit consists of interrupt inputs, an interrupt redirection table, programmable registers, and an APIC bus interface. When an I/O device asserts an interrupt input signal, the IOAPIC selects the corresponding entry in the redirection table, which it uses to format an APIC message for broadcast. Each entry in the redirection table can be individually programmed to indicate edge/level sensitivity, interrupt vector and priority, destination, and static/dynamic processor selection.

Refer to the Intel *82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC), 1996* data book for tables and register descriptions. Intel's web site is http://developer.intel.com/

The major features of the APIC sub-system are listed below.

- 18 individually maskable interrupts
- Jumperless configuration
- Level-triggered or edge-triggered recognition
- Fixed or rotating priorities
- PCI Interrupt support
- PCI Extended Mode register support



APIC Sub-System Functional Block Diagram

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the interrupt inputs.

- Refer to the Intel *82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator* data sheet for more information on the PIIX3 interrupt controller registers. The data sheet is available online at:

  http://developer.intel.com/design/chipsets/datashts/290550.htm

- Refer to the Intel *82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC), 1996* data book for more information on the IOAPIC operating modes. The data sheet is available online at:

  http://developer.intel.com/design/chipsets/datashts/290566.htm

- Refer to the Intel *Architecture Software Developer Manual, Volume 3: System Programming Guide* for more information on the local APIC functions. The data sheet is available online at:

  http://developer.intel.com/design/mobile/MANUALS/243192.htm

- Refer to the Intel *MultiProcessor Specification, version 1.4,* for more information on the multiprocessor interrupt control. The data sheet is available online at:

  http://www.intel.com/design/pentium/datashts/242016.htm

These data sheets are in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

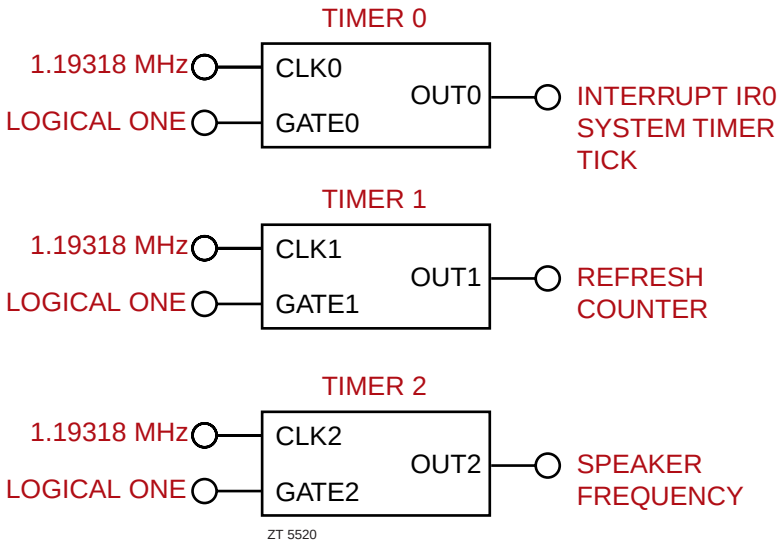
5. COUNTER/TIMERS

The ZT 5520 includes one Intel-compatible 8254 device with a total of three programmable counter/timers, incorporated into the Intel PIIX3 (82371SB) chipset. The counter/timers are useful for software timing loops, timed interrupts, and periodic interrupts.

The major features of the counter/timers are listed below.

- Three 16-bit counter/timers
- Six programmable operating modes
- Binary and BCD counting
- Interrupt and polled operation

The counter/timer architecture is illustrated in the "Counter/Timer Architecture" figure below. In some cases, not all counter/timers are available for application development. In an MS DOS system, for example, counter/timer 0 generates a periodic system interrupt and should not be programmed by the application. Refer to the selected operating system manual for more information.



Counter/Timer Architecture

The six programmable operating modes are summarized in the following table "Counter/Timer Operating Modes".

Counter/Timer Operating Modes

Mode	Counter/Timer Output Operation
0	Transitions after programmed count expires. Gate tied high to enable counting
1	Transitions after programmed count expires. Gate tied high to enable counting
2	Periodic single pulse after programmed count expires. Gate tied high to enable counting
3	Square wave with frequency equal to programmed count. Gate tied high to enable counting
4	Single pulse after programmed count expires. Gate tied high to enable counting
5	Single pulse after programmed count expires. Gate tied high to enable counting

PROGRAMMABLE REGISTERS

The counter/timers are accessed through four I/O addresses as shown in the "Counter/Timer Register Addressing" table below. Each counter/timer occupies an I/O port address through which the preset count values are written and both the count and status information is read. The Control register occupies the remaining I/O port address, which services all three counter/timers.

Counter/Timer Register Addressing

Address	Register	Operation
0040h	Channel 0 Count	Read/Write
0040h	Channel 0 Status	Read
0041h	Channel 1 Count	Read/Write
0041h	Channel 1 Status	Read
0042h	Channel 2 Count	Read/Write
0042h	Channel 2 Status	Read
0043h	Control	Write

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the counter/timers. These manuals are available on Ziatech's web site at http://www.ziatech.com/manuals.htm.

Refer to the Intel *82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator* data sheet for more information on the PIIX3 interrupt controller registers. The data sheet is available online at:

http://developer.intel.com/design/chipsets/datashts/290550.htm

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

6. DMA CONTROLLER

This chapter provides an overview of the ZT 5520 DMA architecture and DMA controller operation. Descriptions of the DMA controller programmable registers are also included.

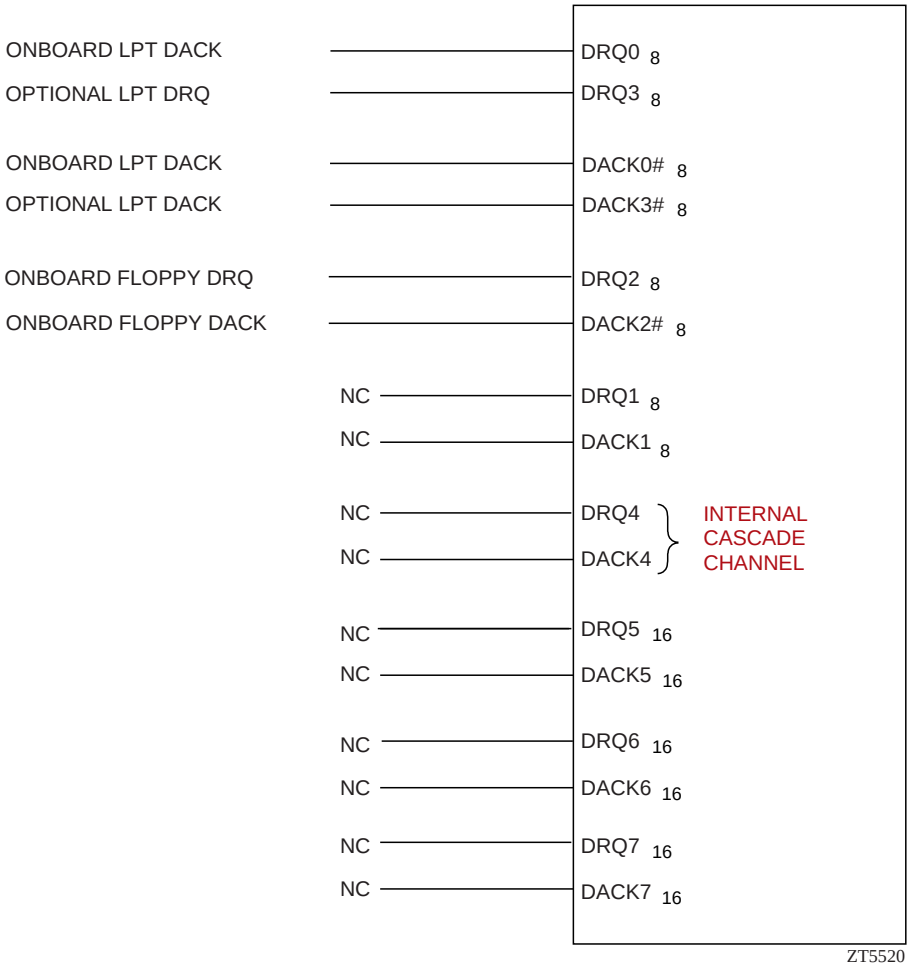
SPECIFICS

The ZT 5520 includes two cascaded, Intel-compatible, 8237 Direct Memory Access controllers that provide a programmable interface for direct transfers between peripherals and main memory. The DMA controllers used on the ZT 5520 are supersets of the 8237 device incorporated into the Intel PIIX3 (82371SB) chipset, supporting 32-bit memory accesses, higher speed transfers, and the PCI protocol. Features of the DMA controllers include:

- 8237 Compatible/superset
- Seven DMA Channel support
- 32-bit memory addressing
- Compatible, TYPE A, TYPE B, TYPE F transfer rates
- Fixed or rotating priorities
- PCI Bus mastering

The DMA architecture is illustrated in the "DMA Architecture" figure.

The on-board IEEE 1234 Parallel Port can be software configured to use DMA channel 0 or 3 for data transfers. The Parallel Port must be configured for ECP mode to use DMA. The optional floppy drive is configured to use DMA channel 2. See Chapter 9, "IEEE-1284 Parallel Port Interface," for more information.



DMA Architecture

PROGRAMMABLE REGISTERS

Each DMA controller is managed through the 16 I/O port addresses shown in the "Slave DMA I/O Port Addressing" table below. Page registers extend the 16-bit DMA address to the full 24-bit address space available on the ZT 5520. I/O port addressing for the DMA page registers is given in the "DMA Page I/O Port Addressing" and the "DMA Extended Page (A24-31) I/O Port Addressing" tables.

Slave DMA I/O Port Addressing

Address			
Slave	**Master**	**Register**	**Operation**
0	C0	Channel 0 Base/Current Address	Write
		Channel 0 Current Address	Read
1	C2	Channel 0 Base/Current Count	Write
		Channel 0 Current Count	Read
2	C4	Channel 1 Base/Current Address	Write
		Channel 1 Current Address	Read
3	C6	Channel 1 Base/Current Count	Write
		Channel 1 Current Count	Read
4	C8	Channel 2 Base/Current Address	Write
		Channel 2 Current Address	Read
5	CA	Channel 2 Base/Current Count	Write
		Channel 2 Current Count	Read
6	CC	Channel 3 Base/Current Address	Write
		Channel 3 Current Address	Read
7	CE	Channel 3 Base/Current Count	Write
		Channel 3 Current Count	Read
8	D0	Status	Read
		Command	Write
9	D2	Write Request	Write
A	D4	Write Single Mask	Write
B	D6	Write Mode	Write
C	D8	Clear Byte Pointer	Write
D	DA	Clear Master	Write
E	DC	Clear Mask	Write
F	DE	Write Mask	Write

DMA Page I/O Port Addressing

Address	Register	Operation
87h	Channel 0 A16-23 Address	Read/Write
83h	Channel 1 A16-23 Address	Read/Write
81h	Channel 2 A16-23 Address	Read/Write
82h	Channel 3 A16-23 Address	Read/Write
8Bh	Channel 5 A16-23 Address	Read/Write
89h	Channel 6 A16-23 Address	Read/Write
8Ah	Channel 7 A16-23 Address	Read/Write

DMA Extended Page (A24-31) I/O Port Addressing

Address	Register	Operation
487h	Channel 0 A24-31 Address	Read/Write
483h	Channel 1 A24-31 Address	Read/Write
481h	Channel 2 A24-31 Address	Read/Write
481h	Channel 3 A24-31 Address	Read/Write
48Bh	Channel 5 A24-31 Address	Read/Write
489h	Channel 6 A24-31 Address	Read/Write
48Ah	Channel 7 A24-31 Address	Read/Write

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the operating system's use of the interrupt inputs.

Refer to the Intel *82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator* data sheet for more information on the DMA controller operating modes. The data sheet is available online at:

http://developer.intel.com/design/chipsets/datashts/290550.htm

Refer to the National Semiconductor® *PC87306 SuperI/O™ Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface* for more information on configuring the ECP DMA channel. The data sheet is available online at:

http://www.national.com/ds/PC/PC87306.pdf

These data sheets are in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

7. REAL-TIME CLOCK

The ZT 5520 includes one Motorola-compatible 146818 real-time clock. The real-time clock provides clock and 100-year calendar information in addition to 242 bytes of CMOS setup static RAM. These functions are battery backed for continuous operation even in the absence of system power. The RAM is used by the operating system BIOS to store configuration information. The major features of the real-time clock are listed below.

- Timekeeping to a 1 second resolution
- 50 bytes of CMOS setup RAM
- Leap year compensation
- Daylight Savings Time compensation
- Periodic, Alarm, and Update Ended interrupts
- Battery backed

PROGRAMMABLE REGISTERS

The real-time clock includes 64 register locations. These registers are accessed through I/O port locations 70h and 71h. A real-time clock register is accessed by first writing the offset address of the register to I/O port location 70h. Data is then transferred to or from the register through I/O port location 71h.

This sequence must be repeated to read the same register a second time. The I/O port addressing for the real-time clock is given in the "Real-Time Clock Register Addressing" table.

The topics that follow illustrate the programmable registers for the real-time clock.

Real-Time Clock Register Addressing

Address Offset	Function	Range
0h	Time-Seconds	0-59
1h	Alarm-Seconds	0-59
2h	Time-Minutes	0-59
3h	Alarm-Minutes	0-59
4h	Time-Hours (12 hour mode)	1-12
4h	Time-Hours (24 hour mode)	0-23
5h	Alarm-Hours	0-23
6h	Day of Week	1-7
7h	Date of Month	1-31
8h	Month	1-12
9h	Year	0-99
Ah-Dh	Register A-D	----
Eh-3Fh	General Purpose	----

ADDITIONAL INFORMATION

Refer to the National Semiconductor® *PC87306 SuperI/O™ Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface* preliminary data sheet for more information on the real-time clock operating modes. The data sheet is available online at:

http://www.national.com/ds/PC/PC87306.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

8. SERIAL CONTROLLER

This chapter discusses the operation of the ZT 5520's two serial ports. Each channel is compatible with the industry standard 16550 serial port, including support for a 16 byte FIFO for read and write operations.

SPECIFICS

The ZT 5520 includes two serial ports that are compatible with the industry standard 16550. The interface for each serial port is implemented with 5 V charge pump technology to eliminate the need for a ±12 V supply. The serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud. Both channels are supplied as DTE configured devices through 9-pin D-Shell connectors (J12 COM2 and J13 COM1) on the front panel, or through the rear-panel user I/O connector J3.

The major features of each serial port are listed below.

- Two RS-232 channels
- 16550 compatible
- Drivers do not require ±12 V
- Baud rates up to 115.2 Kbaud
- Polled and interrupt operation
- Loopback diagnostics

Details for the two serial ports on the ZT 5520 are discussed in the following topics.

Address Mapping

The address mapping for the PC standard architecture and the ZT 5520 is shown below.

Serial Channel	PC Port Address	ZT 5520 Port Address
COM1	3F8-3FF	3F8-3FF
COM2	2F8-2FF	2F8-2FF

Interrupt Selection

The interrupt mapping for the PC standard architecture and the ZT 5520 is shown below.

Serial Channel	PC Interrupt	ZT 5520 Interrupt
COM1	IR4	IR4
COM2	IR3	IR3

Handshake Signals

The PC architecture includes the following handshake signals:

- Transmit Data (TXD)
- Receive Data (RXD)
- Request To Send (RTS)
- Clear To Send (CTS)
- Data Set Ready (DSR)
- Data Terminal Ready (DTR)
- Ring Indicator (RI)
- Data Carrier Detect (DCD)

Serial Channel Interface

The serial ports are configured as DTE and are available through the front panel 9-pin D-shell connectors (J12 COM2 and J13 COM1) or through the rear-panel user I/O connector J3.

PROGRAMMABLE REGISTERS

There are six registers for initializing and controlling each serial channel. The "Serial Controller Register Addressing" table below shows the I/O port addressing for the COM port registers. The topics that follow illustrate the 16-bit divisor latch, baud rate divisors, and the six programmable registers for each serial channel.

Serial Controller Register Addressing

COM 1 Address	COM 2 Address	Register	Operation
03F8h (DIV=0)	02F8h (DIV=0)	Receive Buffer	Read
03F8h (DIV=0)	02F8h (DIV=0)	Transmit Buffer	Write
03F8h (DIV=1)	02F8h (DIV=1)	Divisor Latch LSB	Read/Write
03F9h (DIV=0)	02F9h (DIV=0)	Interrupt Enable	Read/Write
03F9h (DIV=1)	02F9h (DIV=1)	Divisor Latch MSB	Read/Write
03FAh	02FAh	Interrupt Status	Read
03FBh	02FBh	Line Control	Read/Write
03FCh	02FCh	Modem Control	Read/Write
03FDh	02FDh	Line Status	Read
03FEh	02FEh	Modem Status	Read
03FFh	02FFh	Reserved	

ADDITIONAL INFORMATION

Refer to the National Semiconductor *PC87306 SuperI/O™ Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface* preliminary data sheet for more information on the serial controller operating modes. The data sheet is available online at:

http://www.national.com/ds/PC/PC87306.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

9. IEEE-1284 PARALLEL PORT INTERFACE

The ZT 5520 supports an IEEE-1284 compatible printer port interface, available through the rear-panel user I/O connector J3. The printer port can be configured in compatibility, extended, EPP, or ECP modes through the "BIOS SETUP Utility Screen" (discussed in the section "Setup" in Chapter 2).

PARALLEL PORT CONFIGURATION OPTIONS

The different modes for the printer port are described below. Details for the parallel port on the ZT 5520 are discussed in the following topics.

Parallel Port Mode	Description	Max. Data Rate
Compatibility (Default)	Unidirectional data configuration. The original PC-AT Mode. Also known as "nibble mode" because the four status bits in the cable are used for feedback from devices such as tape back-up units (when restoring data from a tape). Software based protocol.	50-150 Kbits/s
Extended	Bi-directional data transfer capability. Similar to Compatibility mode, but allows 8-bit data in both directions. Faster for interfaces needing to supply data to the computer (e.g., scanners, tape back-up). Software based protocol.	50-150 Kbits/s
EPP	Enhanced Parallel Port. Hardware based handshaking of the data transfers provide single I/O instruction data transfers in read and write operations. Register superset of compatibility/extended modes.	500 Kbits/s-2 Mbits/s
ECP	IEEE-1284 Extended Capability Port. Similar to EPP, but register set is strictly defined. Adds FIFOs for read/write operations. ECP devices require IEEE-1284 compliant cabling and buffers. The ZT 5520 supplies compliant buffers - cabling is available from other sources.	500 Kbits/s-2 Mbits/s

ADDRESS MAPPING

The address mapping for the PC standard architecture and the ZT 5520 is shown below.

Parallel Port	PC Port Address	ZT 5520 Port Address
LPT1	3BC (typically)	378-37F - Compatibility, Extended, EPP Modes 378-37A, 778-77A - ECP Mode

INTERRUPT SELECTION

The interrupt mapping for the PC standard architecture and the ZT 5520 is shown below.

Parallel Port	PC Interrupt	ZT 5520 Interrupt
LPT1	IR5 or IR7	IR7

DMA SELECTION

DMA may be configured for ECP mode in software. DMA channel 0 is dedicated for ECP support and may be used by application software. The BIOS does not use DMA for any data transfers. Applications needing DMA support must configure the parallel port with appropriate initialization code.

PROGRAMMABLE REGISTERS

There are three registers for the compatibility/extended mode parallel port interface. The "Compatibility/Extended Mode Parallel Port Interface Addressing" table below shows the I/O port addressing. For EPP and ECP information, consult the *National Semiconductor PC87303* data sheet.

Compatibility/Extended Mode Parallel Port Interface Addressing

Address	Register	Operation
0378h	Line Printer Data	Read/Write
0379h	Line Printer Status	Read
037Ah	Line Printer Control	Read/Write

ADDITIONAL INFORMATION

Refer to the National Semiconductor *PC87306 SuperI/O™ Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface* preliminary data sheet for more information on the parallel controller operating modes. The data sheet is available online at:

http://www.national.com/ds/PC/PC87306.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

The IEEE-1284 specification (document #DS02709) can be obtained from the IEEE Standards Office at (800) 678-4333. Their web site is http://ieee.com.

10. OPTIONAL FLOPPY DISK INTERFACE

This chapter provides an overview of the Floppy Disk Controller. It includes a list of product features and discusses enabling an optional floppy disk interface.

FEATURES OF THE OPTIONAL FLOPPY DISK INTERFACE

- 360 Kbyte, 720 Kbyte, 1.2 Mbyte, and 1.44 Mbyte floppy disk drive support
- IBM®-PC®/AT®/MCA®/EISA® compatible register set
- 3½" floppy disk drive support
- Integrated 3½" slimline floppy disk drive (1 slot usage)

INTERRUPTS

The Floppy Disk Controller (FDC) communicates status to the host processor via interrupt IRQ6.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller supports all DOS-compatible floppy disk drives through the rear-panel user I/O connector (J3). Data rates of 250 Kbytes, 300 Kbytes, 500 Kbytes, and 1 Mbits/s are supported through program control. An on-board 16-byte FIFO provides increased bus-latency tolerance. The FDC is fully compatible with the IBM-AT, IBM-PS/2®, and EISA architectures.

Connector J3 provides a mechanism for the floppy drive to be remotely mounted (via a rear-panel transition board), or accessed on the ZT 5980 System Utility Board connected to the CompactPCI backplane. The ZT 5980 provides a 3.5" slimline floppy drive and optional hard drive for development system or target applications.

DMA CHANNEL

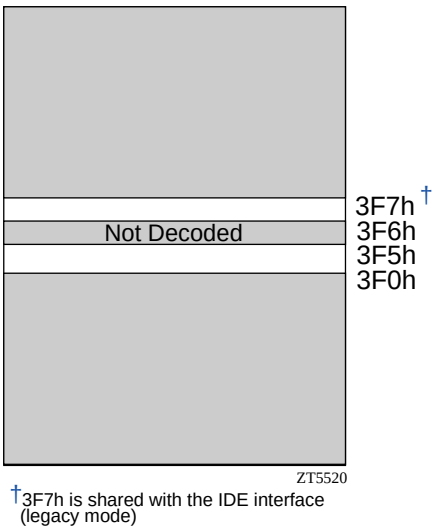
The optional floppy drive is configured to use DMA channel 2.

MEMORY

The floppy interface does not occupy or decode any memory address space.

I/O

The floppy interface I/O address range is 3F0h-3F7h, excluding 3F6h. Port 3F7h is shared with the hard disk interface. The "Floppy Disk I/O Map" is shown below.



Floppy Disk I/O Map

DATA TRANSFERS

The floppy disk controller supports both polled and DMA-driven data transfers. Standard MS-DOS uses DMA, by default, for moving data back and forth between the host CPU's memory and the floppy disk controller. The DMA transfer is driven by the DMA controller on board the CPU board. The BIOS software is responsible for managing the low-level hardware in DOS systems. All transfers are 8 bits wide.

ADDITIONAL INFORMATION

Refer to the National Semiconductor *PC87306 SuperI/O™ Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface* preliminary data sheet for more information on the optional floppy disk controller operating modes. The data sheet is available online at:

http://www.national.com/ds/PC/PC87306.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

11. SYSTEM REGISTERS

Two system registers are used to control and monitor a variety of functions on the ZT 5520. The system registers are read/write capable. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under their control.

Note that where switches are referenced in this chapter, "SWx" corresponds to the switch number and "-N" corresponds to the switch position (for example, SW4-2 means "switch number 4, position 2").

SYSTEM REGISTER DEFINITION

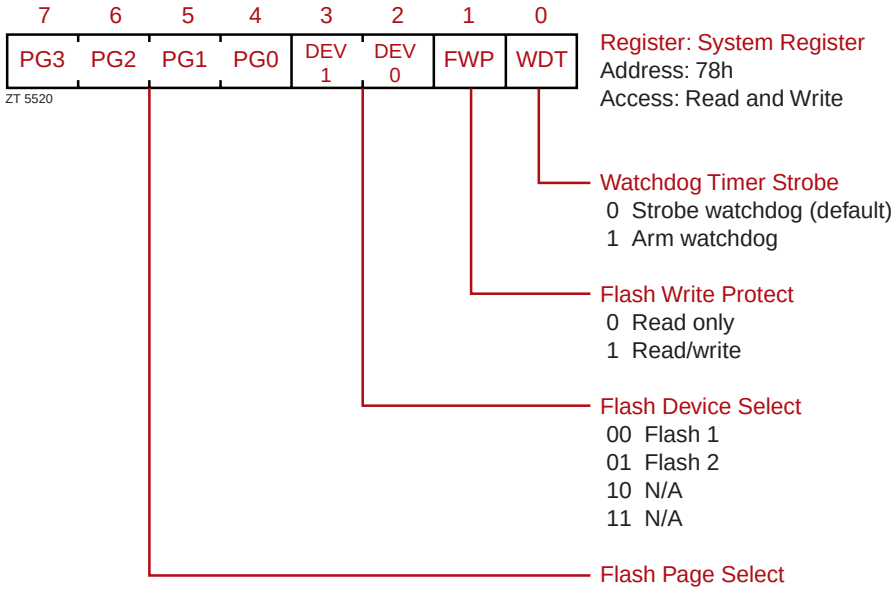
The System registers can be accessed at I/O port 78h. Refer to the "System Register" illustration below.

Bit 0 is used for arming the watchdog timer. See the "Watchdog Timer Operation" section in Chapter 12 for more information on using this bit.

Bit 1 is the flash write-protect bit. The BIOS and STD.SYS ensure that the flash is protected from random writes. SW4-4 is used to absolutely protect the flash.

Bits 2-3 are the device select bits.

Bits 4-7 are the page select bits.



System Register

DIGITAL I/O ASIC DEFINITIONS

In addition to the System register, the ZT 5520 uses several ports of the on-board 16C50A Digital I/O ASIC device for monitoring and controlling other board functions. These registers are mapped to I/O ports E1h through E5h. Descriptions of these registers are given in the following topics.

For more information on how the Digital I/O ASIC works, refer to the section "Functional Description" section in Chapter 13, "Parallel I/O".

Refer to Appendix C, "Digital I/O ASIC System Setup Considerations," for tips on preventing latchup from the CMOS parts in the 16C50A.

Note that the Digital I/O ASIC inputs are inverting; thus, a logic high (+5 V) will be read as a logic low (0 V).

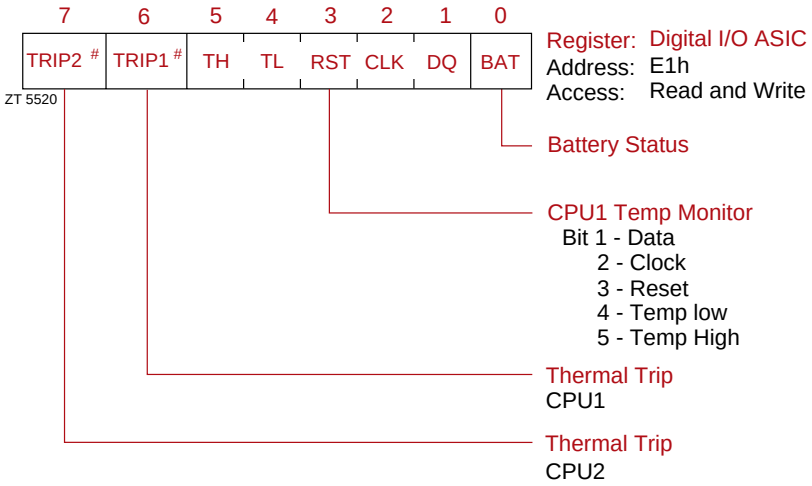
Digital I/O ASIC (Port E1h)

This register is illustrated in the "Digital I/O ASIC (Port E1h)" figure.

Bit 0: Battery Status. This input is not implemented on the current revision of the ZT 5520.

Bit 1 - Bit 5: Temperature Monitor (CPU1).These bits are used to control the on-board temperature monitor for CPU1. See the "Temperature Monitoring" section in Chapter 15 for more information on using this feature.

Bit 6 - Bit 7: CPU Thermal Trip. These bits are set in the event that one of the CPU cores exceeds 130º C. Cuttable traces CT22 and CT33 must be in (default) for the CPU's THERMTRIP# signal to be monitored by these bits.



Digital I/O ASIC (Port E1h)

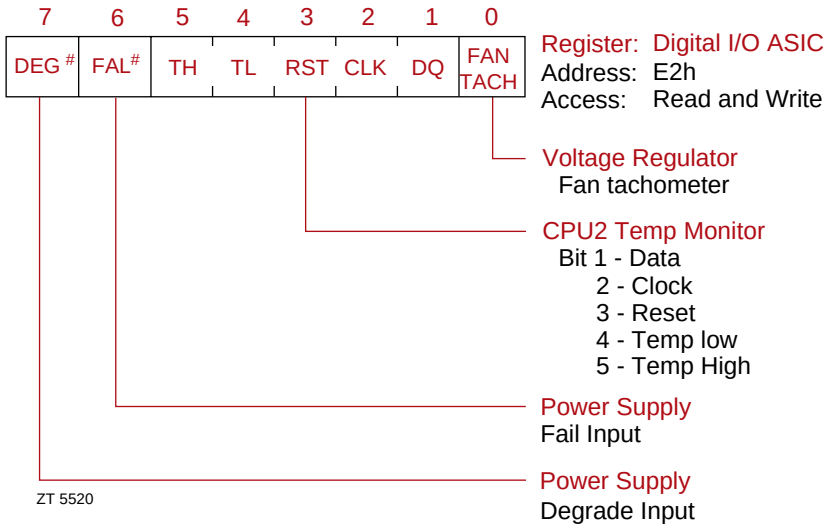
Digital I/O ASIC (Port E2h)

This register is illustrated in the "Digital I/O ASIC (Port E2h)" figure below.

Bit 0: Voltage Regulator Fan Tachometer. This bit is used to monitor a fan with a tachometer output. This input is connected to J11, pin 3, via a watchdog timer. The factory installed fan does not have a tachometer output.

Bit 1 - Bit 5: Temperature Monitor (CPU2). These bits are used to control the on-board temperature monitor for CPU2. See the "Temperature Monitoring" section in Chapter 15 for more information on using this feature.

Bit 6 - Bit 7: Power Supply DEG#, FAL#. These bits monitor the DEG# and FAL# signals on CompactPCI connectors J1 and J4.



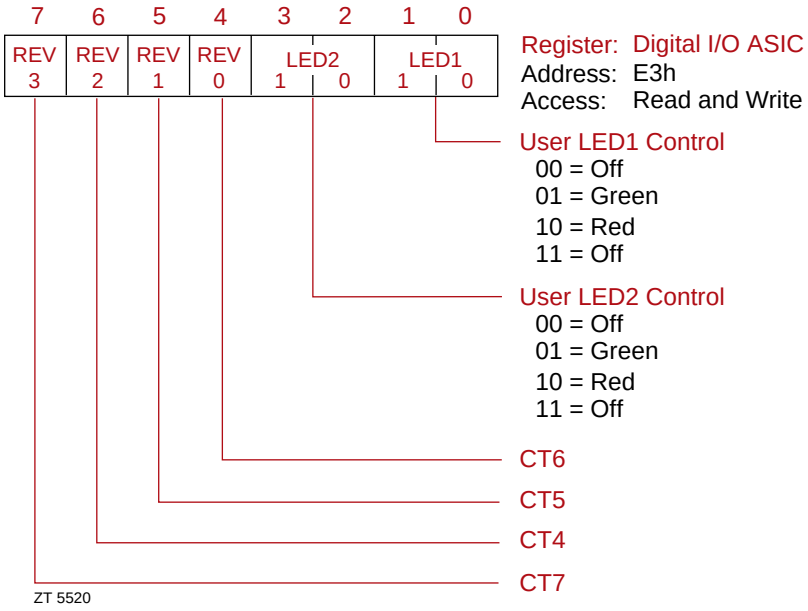
Digital I/O ASIC (Port E2h)

Digital I/O ASIC (Port E3h)

This register is illustrated in the "Digital I/O ASIC (Port E3h)" figure below.

Bit 0 - Bit 3: On-Board User LED Control. (See Chapter 14, "Programmable LED," for more information).

Bit 4 - Bit 7: Major Board Revision. This port is used to read the status of cuttable traces CT4 - CT7 to determine the current board revision. Revisions A, B, and C = xFh. The user should not change these cuttable traces since this value may be used by the system BIOS. See the "Cuttable Trace Options And Locations" section in Appendix A for more information on cuttable traces.



Digital I/O ASIC (Port E3h)

Digital I/O ASIC (Port E4h)

This register is illustrated in the "Digital I/O ASIC (Port E4h)" figure below.

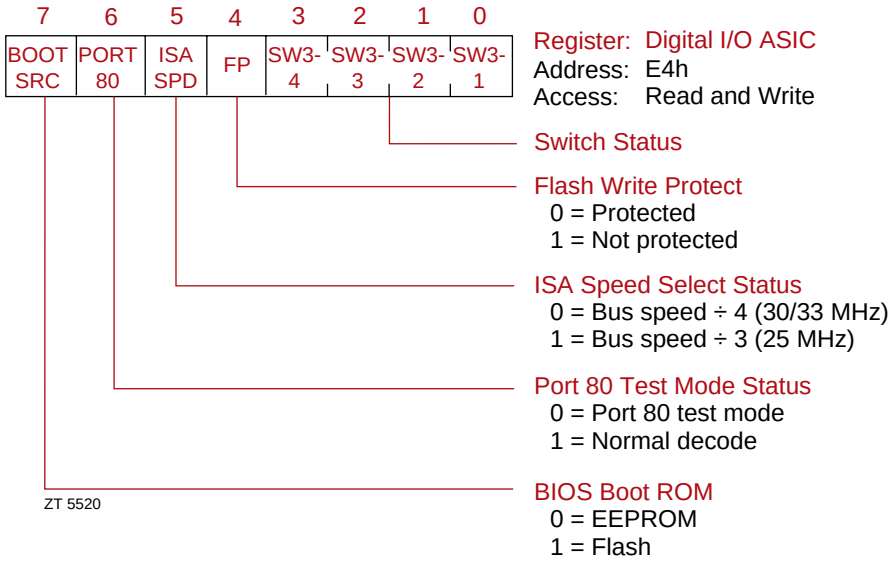
Bit 0 - Bit 3: Software Configuration. These bits are used to provide configuration information to the user's software by monitoring the status of switch SW3, located on the solder side of the ZT 5520.

Bit 4: Flash Protect Status. This bit corresponds to the status of switch SW4-4. See the "Switch Descriptions" section in Appendix A for more information.

Bit 5: ISA Speed Select Status. This bit corresponds to the status of switch SW4-3. See the "Switch Descriptions" section in Appendix A for more information.

Bit 6: Port 80 Test Mode Status. This bit corresponds to the status of switch SW4-2. See the "Switch Descriptions" section in Appendix A for more information.

Bit 7: Boot Source Status. This bit corresponds to the status of switch SW4-1. See the "Switch Descriptions" section in Appendix A for more information.



Digital I/O ASIC (Port E4h)

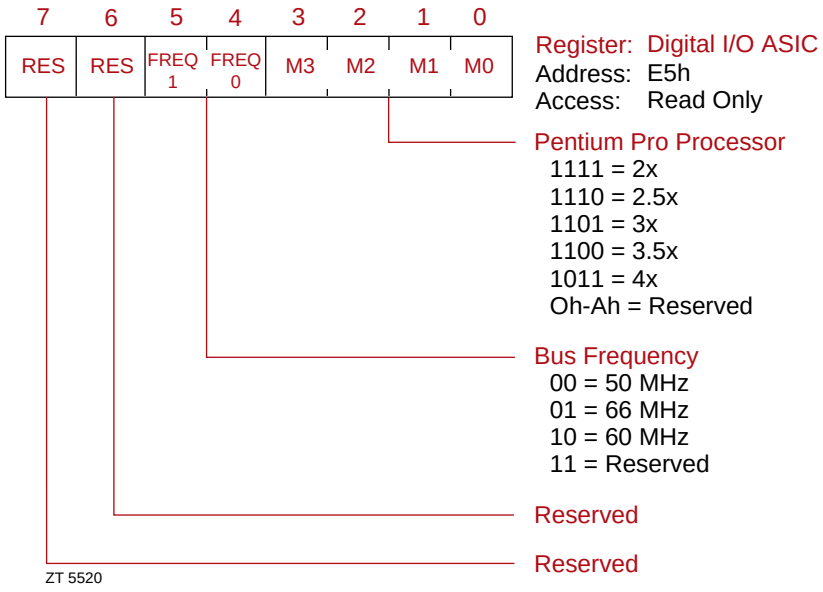
Digital I/O ASIC (Port E5h)

This register is illustrated in the "Digital I/O ASIC (Port E5h)" figure below.

Bit 0 -- Bit 3: Pentium Pro Multiplier Status. These bits correspond to the status of the processor core frequency multiplier strapping. See the "CPU Multiplier Settings" table in Appendix A for more information.

Bit 4 - Bit 5: CPU Bus Frequency Status. These bits correspond to the status of cuttable traces CT42 and CT43, respectively. See the "Cuttable Trace Options And Locations" section in Appendix A for more information on cuttable traces.

Bit 6 - Bit 7: Reserved. These are reserved for future use and should not be changed by the user.



Digital I/O ASIC (Port E5h)

12. WATCHDOG TIMER

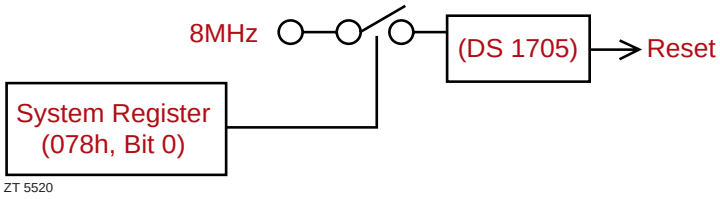
The primary function of the watchdog timer is to monitor ZT 5520 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are listed below.

- Single-stage
- Enabled and disabled through software control
- Armed and strobed through software control

WATCHDOG TIMER OPERATION

The watchdog timer architecture is illustrated in the "Watchdog Timer Architecture" figure below. The watchdog timer is implemented in the Dallas Semiconductor™ DS1705 system monitor. After power on or reset, the watchdog function is disabled, meaning that the watchdog is continually being strobed by an 8 MHz signal. **Bit 0** of the System Register (078h) must be programmed with a logical 1 to enable the watchdog timer to begin operation.

If the watchdog is allowed to expire, a reset is generated. To strobe the watchdog, bit 0 of the System Register (078h) must be written with a logical 0 and then a logical 1.The watchdog timeout period is fixed at 1.0 s minimum and 2.2 s maximum. Software must strobe the watchdog timer within 1.0 s to guarantee that the system is not reset.



Watchdog Timer Architecture

ADDITIONAL INFORMATION

Refer to the Dallas Semiconductor *DS1705/DS1706 3.3 and 5.0 Volt Micromonitor* data sheet for more information on the watchdog timer and the associated operating modes. The data sheet is available online at:

http://www.dalsemi.com/DocControl/PDFs/1705-06.pdf

Refer to the Intel *82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator* data sheet for more information on the PIIX3 Reset Control register. The data sheet is available online at:

http://developer.intel.com/design/chipsets/datashts/290550.htm

These data sheets are in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

13. PARALLEL I/O

The ZT 5520 includes six 8-bit parallel ports for a total of 48 I/O signals. One of the parallel ports is available to the user through connector J17. The remaining five parallel ports are dedicated to controlling and monitoring local operations. The general operation of the six parallel ports is explained in this chapter. The specific features managed by the dedicated ports are explained in Chapter 11, "System Registers".

Each of the parallel I/O signals is configured as an input or an output with readback under software control. The major features of the parallel I/O are listed below.

- 12 mA sink current
- Software programmable input debounce
- Stable outputs during power up and reset
- Continuous data transfer rates up to 1 Mbyte/second
- Software programmable event sense interrupt generation

FUNCTIONAL DESCRIPTION

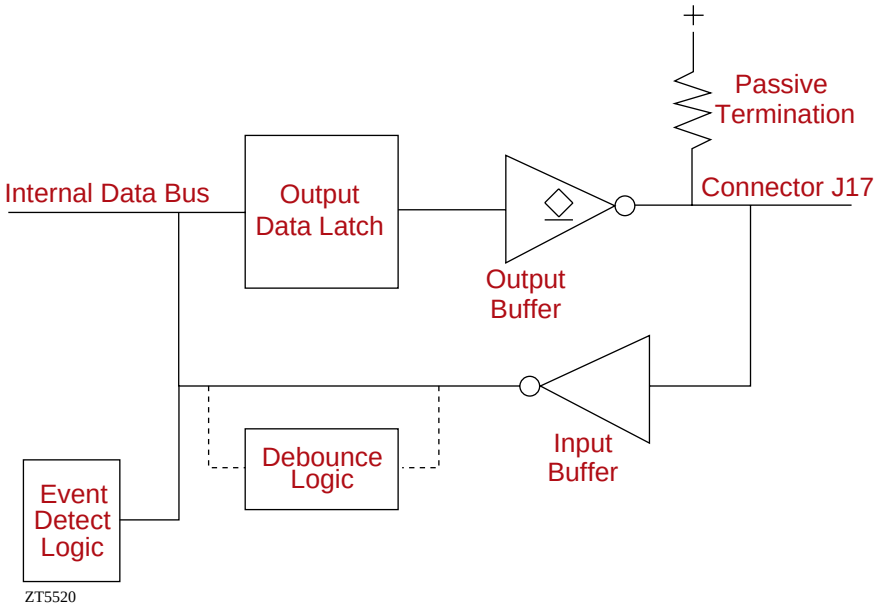
The parallel I/O signals are supported through the 16C50A Digital I/O ASIC, a custom ASIC device designed by Ziatech.

The 16C50A Digital I/O ASIC supports **standard** and **enhanced** operating modes. Enhanced operating mode is configured by the ZT 5520 BIOS. There are three register banks (see "Programmable Registers" later in this chapter) used for controlling the device's features. These register banks are selected by programming bits 6 and 7 of I/O port E7h with a "00" for **bank 0**, a "01" for **bank 1**, and a "10" for **bank 2**.

The "Parallel Port Functional Diagram" shows the internal circuitry of each I/O signal. The diagram includes an output latch, an output buffer, and an input buffer. These functional blocks are described in the following topics.

Refer to Appendix C, "Digital I/O ASIC System Setup Considerations," for tips on preventing latchup from the CMOS parts in the 16C50A Digital I/O ASIC.

Several ports of the on-board 16C50A Digital I/O ASIC device are used for monitoring and controlling other board functions. See the section, "Digital I/O ASIC Definitions," in Chapter 11 for more information.



Parallel Port Functional Diagram

Output Latch

The output latch stores the data present on the internal data bus during a write operation to the parallel port. The data is latched until altered by another parallel port write, until a system reset, or until the power is turned off. The output latch is initialized with a logical 0 during power on and system reset.

Output Buffer

The output buffer isolates the output latch from connector J17. The output buffer is an inverting open-collector device with 12 mA of sink current and glitch-free operation during power cycles. The inversion means that a logical 0 written to the parallel port appears as a TTL high at connector J17, and a logical 1 written to the parallel port appears as a TTL low at connector J17.

The open collector feature permits each parallel I/O signal to be software configured as an input. To use a parallel port signal as an input, a logical 0 must first be written to the output latch. This causes the output buffer to become an open-collector gate and prevents contention with the input signal. The passive termination ranges from 25k ohms minimum to 120k ohms maximum. Applications needing a predictable rise time should provide additional termination.

Input Buffer

The input buffer is enabled during read operations to transfer the data from the Digital I/O ASIC pins to the internal data bus. If the parallel port bit is configured as input, the data read is the data driven by an external device.

The input buffer is an inverting device. This means that data read from the parallel port as a logical "0" is a TTL high at connector J17, and data read from the parallel port as a logical "1" is a TTL low at connector J17.

Debounce Control Logic

The debounce control logic is a new feature of the 16C50A Digital I/O ASIC. This feature eliminates the need for external logic or extensive software to remove unstable input signals to the Digital I/O ASIC. The internal circuitry of the Digital I/O ASIC automatically filters out glitches that can occur in received signals.

For example, if the Digital I/O ASIC is programmed for an 8 ms period, the incoming signal must be stable for the entire 8 ms period, with no glitches, before it is recognized by the Digital I/O ASIC.

The debounce control logic is controlled on the 16C50A by registers E0h, E1h, E2h, and E3h in register bank 2. An 8 MHz clock is used by the 16C50A for a timing reference, thus allowing the debounce circuit to be programmed for a debounce delay of 4 µs, 64 µs, 1 ms, or 8 ms.

Upon initialization of the debounce circuitry, be sure to delay at least the programmed debounce time before reading any of the input ports or the external event signals. This guarantees that the input data is valid prior to being used by the software.

Event Sense Detection Logic

The 16C50A Digital I/O ASIC contains event sense logic that allows the detection of either positive or negative events. The event input edge is controlled on a nibble basis by software. The event bits are enabled on an individual basis. Registers E0-E6h in register bank 1 are used to control and monitor the event sense logic. The Event Sense interrupt (optionally assigned to IRQ5) is not supported with the standard ZT 5520 BIOS. Contact Ziatech for more information if this feature is required.

To use the event inputs:

1. Determine which events are to be enabled and what polarity is to be detected, high to low (negative) or low to high (positive) transitions.
2. Set each port to the desired polarity.
3. Enable each of the event inputs to be detected.

All I/O and external event inputs are reset to negative events, and disabled after a Reset signal has occurred.

PROGRAMMABLE REGISTERS

The 16C50A Digital I/O ASIC supports **standard** and **enhanced** operating modes. Enhanced operating mode is configured by the ZT 5520 BIOS. There are three register banks (listed below) used for controlling the device's features. These register banks are selected by programming bits 6 and 7 of I/O port E7h with a "00" for **bank 0**, a "01" for **bank 1**, and a "10" for **bank 2**. The six 8-bit ports are allocated as follows.

- Enhanced Bank 0 I/O Port Addressing
- Enhanced Bank 1 I/O Port Addressing
- Enhanced Bank 2 I/O Port Addressing
- The I/O port at E0h is available through connector J17 (refer to Appendix B for the J17 connector pin assignments).
- The five I/O ports at E1h, E2h, E3h, E4h, and E5h are dedicated to managing functions local to the ZT 5520. Refer to Chapter 11, "System Registers," for additional information.

Enhanced Bank 0 I/O Port Addressing

Select this register bank by programming bits 6 and 7 of I/O port E7h with a "00".

Address	Register	Read Operation	Write Operation
00E0h	Port 0 Data	DIGIO0-DIGIO7	DIGIO0-DIGIO7
00E1h	Port 1 Data	System Register	System Register
00E2h	Port 2 Data	System Register	System Register
00E3h	Port 3 Data	System Register	System Register
00E4h	Port 4 Data	System Register	System Register
00E5h	Port 5 Data	System Register	System Register
00E6h	Reserved	-----	-----
00E7h	Write Inhibit/ Bank Address	Status	Control

Enhanced Bank 1 I/O Port Addressing

Select this register bank by programming bits 6 and 7 of I/O port E7h with a "01".

Address	Register	Read Operation	Write Operation
00E0h	Port 0 Event Sense	Status	Control
00E1h	Port 1 Event Sense	Status	Control
00E2h	Port 2 Event Sense	Status	Control
00E3h	Port 3 Event Sense	Status	Control
00E4h	Port 4 Event Sense	Status	Control
00E5h	Port 5 Event Sense	Status	Control
00E6h	Event Sense Manage	Status	Control
00E7h	Bank Address	Status	Control

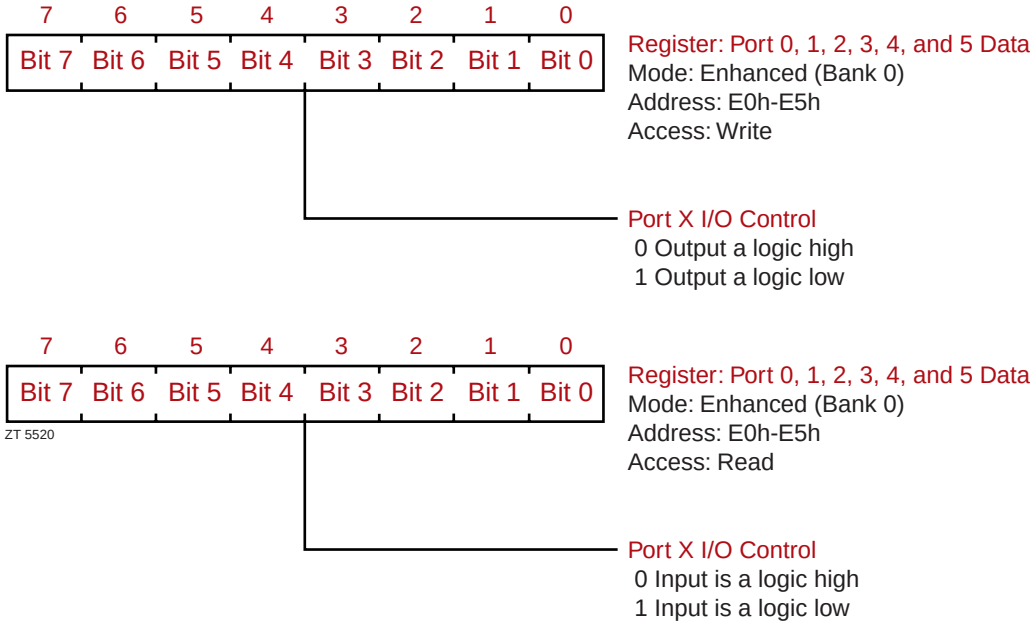
Enhanced Bank 2 I/O Port Addressing

Select this register bank by programming bits 6 and 7 of I/O port E7h with a "10".

Address	Register	Read Operation	Write Operation
00E0h	Debounce Configure	Status	Control
00E1h	Debounce Duration	Status	Control
00E2h	Debounce Duration	Status	Control
00E3h	Debounce Clock	-----	Control
00E4h	Reserved	-----	-----
00E5h	Reserved	-----	-----
00E6h	Reserved	-----	-----
00E7h	Bank Address	Status	Control

Port Data Registers

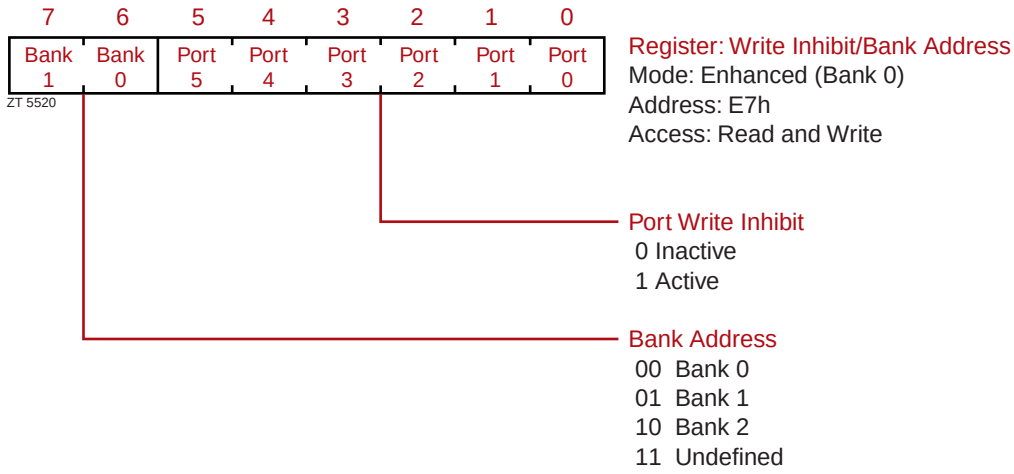
Note: To set a particular port and bit as an input, write a logic 0 to that port and bit.



Parallel Port Data Registers

The six I/O ports assign the least significant I/O line to the least significant data line (D0). Each bit is changed or monitored by writing or reading the individual I/O port. On a power up or reset, the ports are reset to 0, forcing the outputs to be set high.

Write Inhibit / Bank Address Register

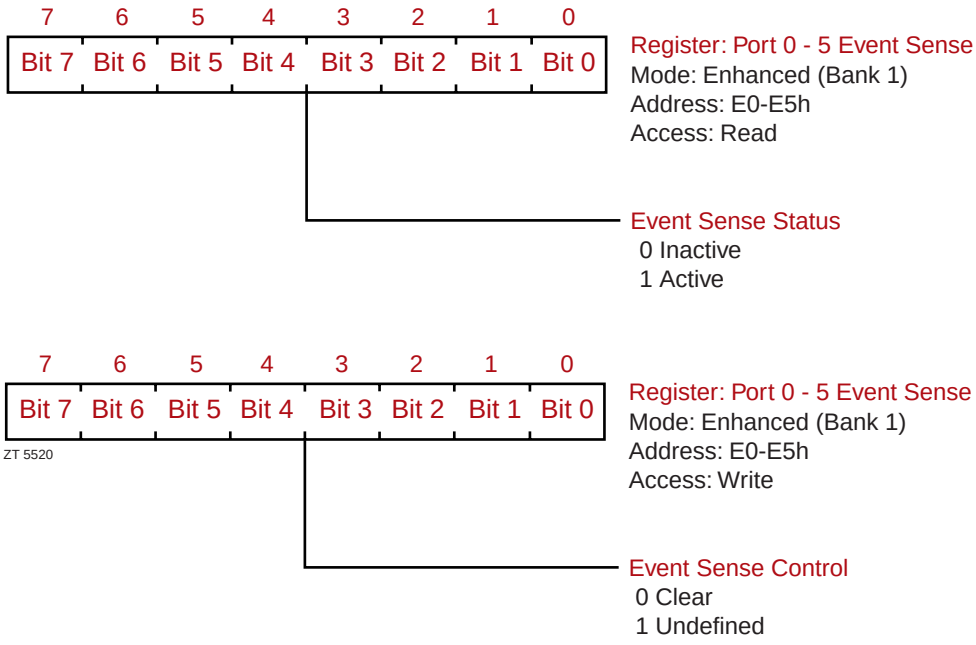


Parallel Port Write Inhibit / Bank Address Register

The Write Inhibit/Bank Address register is used to mask the ability to write data to the six output ports. Power-up default has the register unmasked to allow writes to the output ports. Writing the Write Inhibit/Bank Address register bits D0-5 with a 1 masks I/O ports 0 - 5, respectively, while a read returns the status of the mask register.

Bits 7 and 6 of the register select which bank of registers is selected. A logic 00 selects bank 0, a 01 selects bank 1, and 10 selects bank 2, respectively. A logic 11 is an invalid state and should never be written to the Write Inhibit/Bank Address Register.

Port Event Sense Register

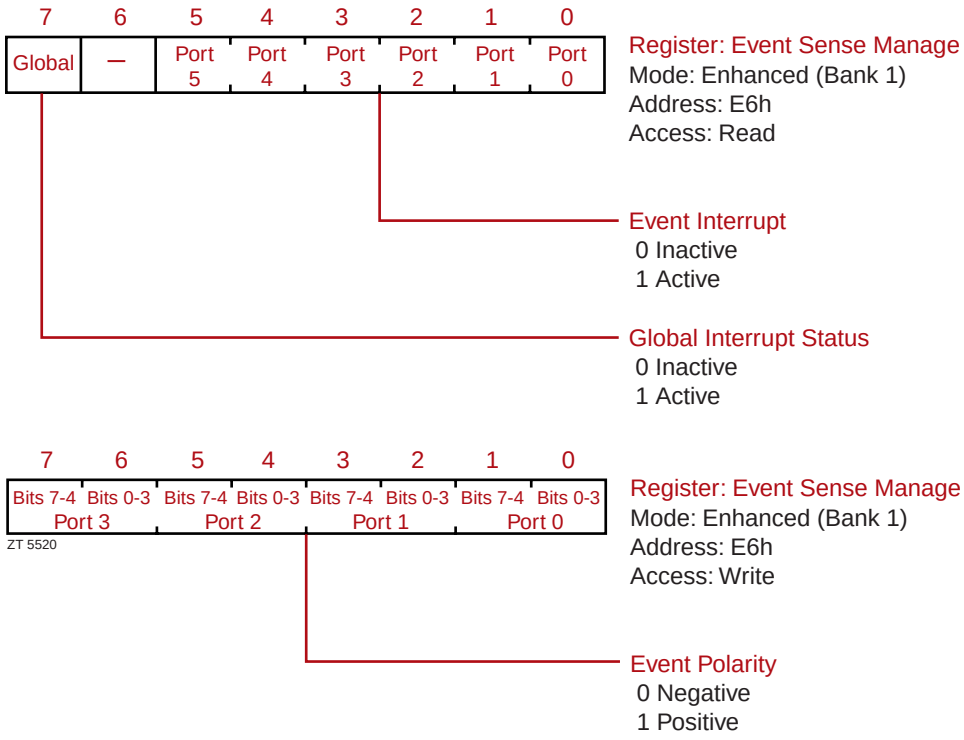


Parallel Port Event Sense Register

Reading the event sense status of each port gets the status of each I/O port sense line. Writing to the event sense status of each port with the corresponding bit equal to 0 clears that particular sense line.

When writing ports 0 - 5, each data bit written with a logic 0 clears its corresponding event sense flip-flop. Each data bit of ports 0 - 5 must be written with a 1 to re-enable the corresponding event sense input after it is cleared. Reading ports 0 - 5 returns the event sense flip-flop status.

Event Sense Manage Register



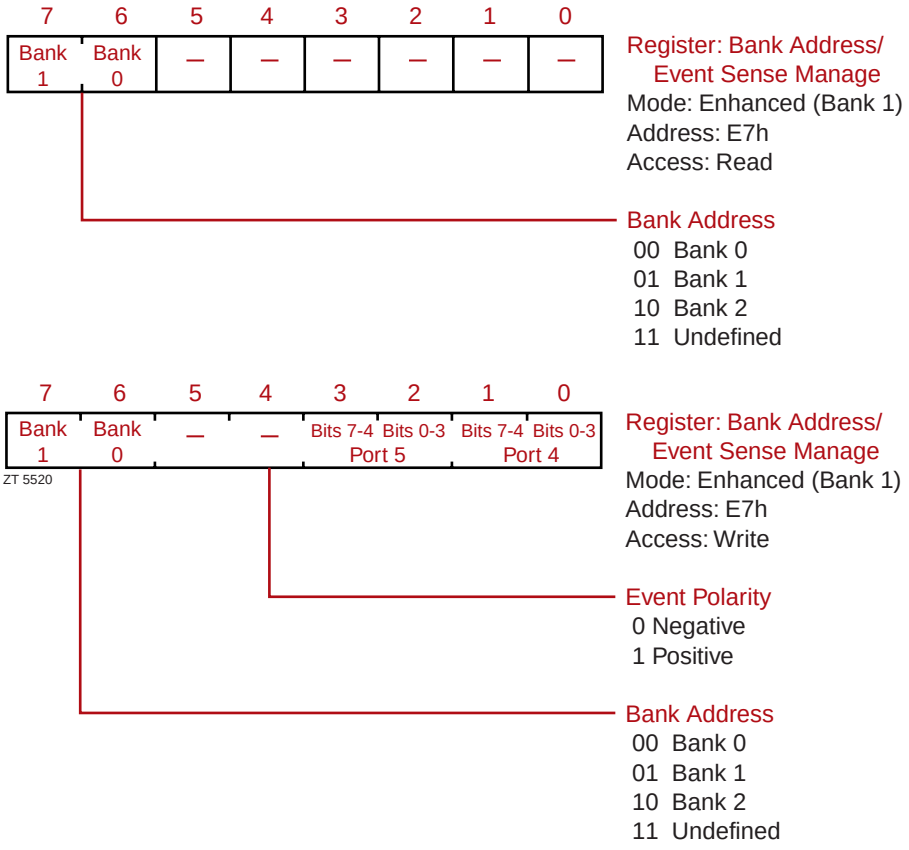
Parallel Port Event Sense Manage Register

A write to this register controls the polarity of the Sense Event for I/O ports 0 - 3. Each bit represents a nibble (4 bits) of the port. A logic 0 senses negative events, while a 1 senses positive events. The polarity of the event sense logic must be set prior to enabling the event input logic.

A read from this register returns the event status on I/O ports 0 - 5 and the status of the interrupt pin.

Bit 7, the global interrupt pin, indicates an event sense was detected on any of the six ports (1 = interrupt is asserted).

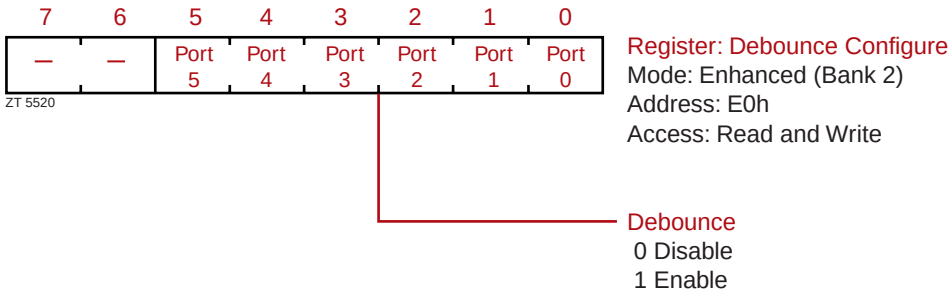
Bank Address Register



Parallel Port Bank Address Register

This register controls the polarity of the Sense Event for I/O ports 4 and 5. A 0 senses negative events, while a 1 senses positive events. Bits 6 and 7 select an individual bank. A read from this register returns only the bank status information.

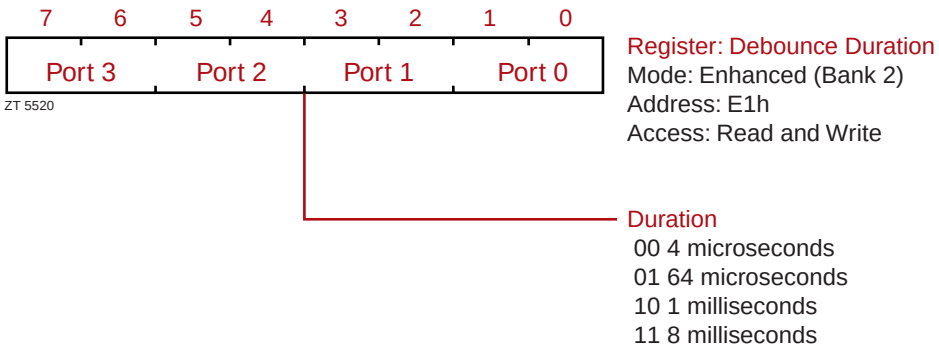
Debounce Configure Register



Parallel Port Debounce Configure Register

This register controls whether each individual port is passed through the debounce logic. A logic 0 disables the debounce logic, and a logic 1 enables the debounce logic.

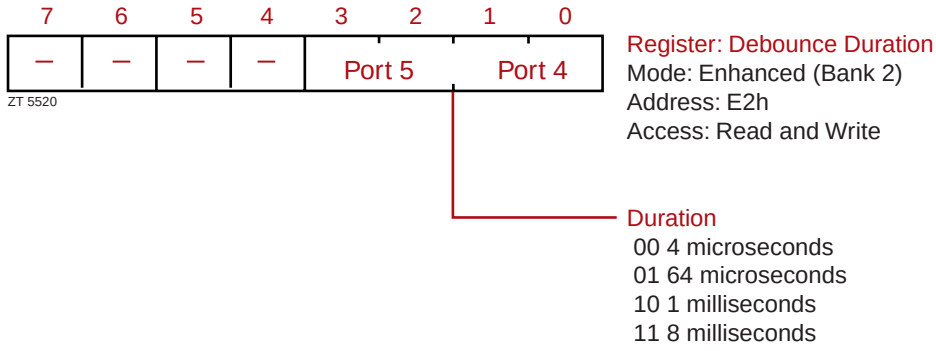
Debounce Duration Register (Ports 0-3)



Parallel Port Debounce Duration Register (Ports 0-3)

This register controls the duration required by each input signal before it is recognized for ports 0 - 3. The debounce times available are 4 µs, 64 µs, 1 ms, and 8 ms. A debounce value of 00 sets 4 µs, 01 sets 64 µs, 10 sets 1 ms, and 11 sets 8 ms. The default value is 00 for a 4 µs debounce period.

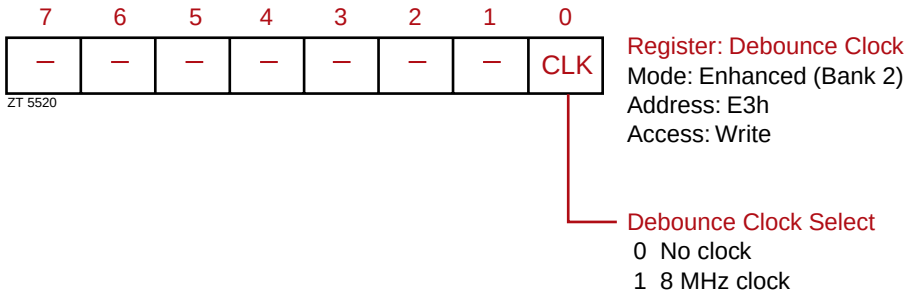
Debounce Duration Register (Ports 4-5)



Parallel Port Debounce Duration Register (Ports 4-5)

This register controls the duration required by each input signal before it is recognized for ports 4 and 5. The debounce times available are 4 µs, 64 µs, 1 ms, and 8 ms. A debounce value of 00 sets 4 µs, 01 sets 64 µs, 10 sets 1 ms, and 11 sets 8 ms. The default value is 00 for a 4 µs debounce period.

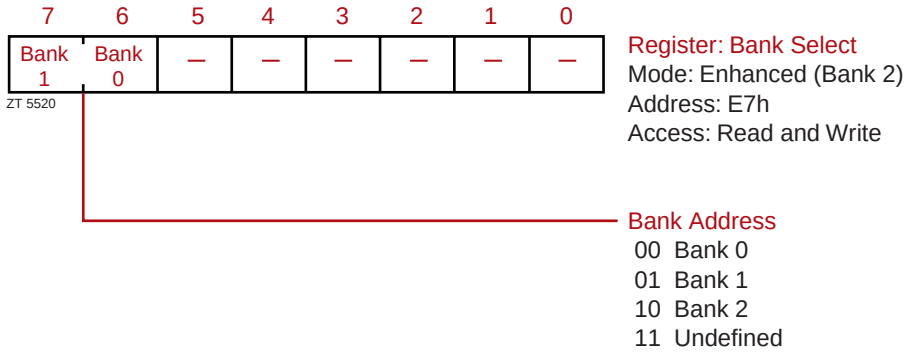
Debounce Clock Register



Parallel Port Debounce Clock Register

This bit must be set to a 1 to use the debounce feature. The default value is 0. A read from this port is undefined.

Bank Select Register



Parallel Port Bank Select Register

14. PROGRAMMABLE LED

The ZT 5520 includes two user controlled bi-color (red/green) Light-Emitting Diodes (LEDs) located on the front panel. The user LEDs are software programmable through **Bits 0-3** of the "Digital I/O ASIC (Port E3h)". The LEDs are turned off after a power cycle or a reset.

Two bits are used to control the state of each LED. Bits 0 and 1 are used for the bottom LED and bits 2 and 3 are used for the top LED. Since bi-color LEDs are used, there are 3 states for each LED: GREEN, RED, and OFF. The LEDs are programmed as follows:

LED	**S T A T E**			
	GREEN	**RED**	**OFF**	**OFF**
Top LED (UD2)				
Bit 2	0	1	1	0
Bit 3	1	0	1	0
Bottom LED (UD1)				
Bit 0	0	1	1	0
Bit 1	1	0	1	0

The LED bits are in the same register as other functions; therefore it is important to preserve the state of the other bits in this register when modifying the LED status. The following code demonstrates the mechanism for modifying the LED bit:

```
; set bottom LED ON (RED)

     cli                ; clear interrupts

     in     al, E3h     ; read current state

     and   al, FCh      ; clear LED bits

     or     al, 01h     ; set LED bits

     out    E3h, al     ; output new value for register

     sti                ; re-enable interrupts


     ; set LED OFF

     cli                ; clear interrupts

     in     al, E3h     ; read current state

     and  al, FCh       ; clear LED bits

     out    E3h, al     ; output new value for register

     sti                ; re-enable interrupts
```

15.THERMAL CONSIDERATIONS

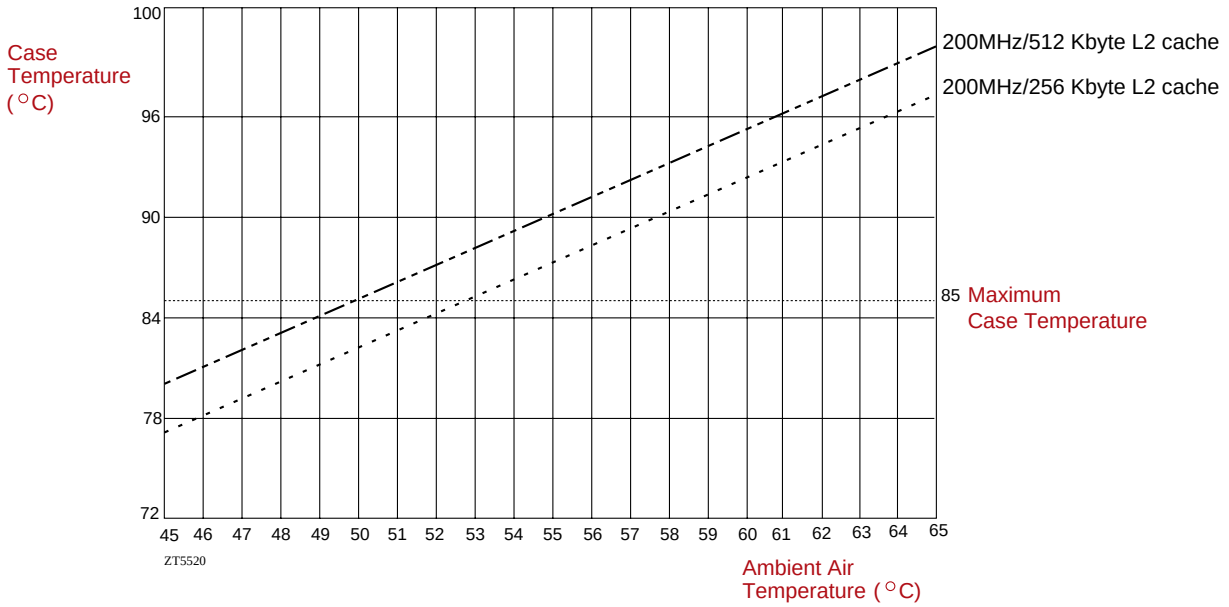
The ZT 5520 comes from the factory with an integrated fan/heatsink for cooling each processor. The fan/heatsink (available through connectors J16 and J20; voltage configured through CT30) allows a maximum ambient air temperature of 52.8º C for the 200 MHz/256 K L2 cache Pentium Pro processor. See the "Pentium Pro Processor Maximum Ambient Temperature" table below.

Pentium Pro Processor Maximum Ambient Temperatures

Processor Speed (MHz/Kbytes L2)	Max. Ambient Temperature (°C)
200/256	52.8
200/512	50.0

The figure below "Ambient Temperature Vs. Pentium Pro Processor Case Temperature" shows the relationship between ambient temperature and case temperature (when operated with the integrated fan/heatsink) for the processor sold with the ZT 5520.

The ZT 5520 is also equipped with a front panel Voltage Regulator Module (VRM) cooling fan (available through connector J11; voltage configured through CT1) for cooling the on-board processor core voltage supplies. This fan is necessary for the proper operation of the voltage supplies and must not be removed. The fan operates at 12 VDC and is rated at 0.7 W. For proper cooling of the ZT 5520, ensure that airflow is not obstructed.



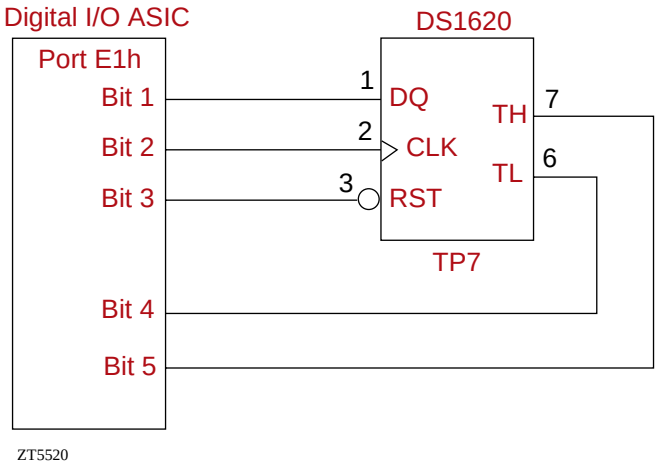
Ambient Temperature Vs. Pentium Pro Processor Case Temperature

TEMPERATURE MONITORING

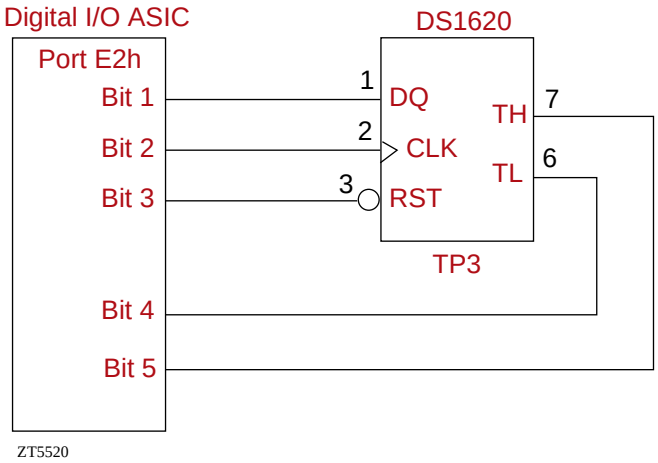
The ZT 5520 contains two on-board thermal sensors to monitor processor temperature:

- The sensor for **CPU1** is accessed by **Bits 1-5** of the "Digital I/O ASIC (Port E1h)." Connection of the thermal sensor for **CPU1** is shown in the "CPU1 Thermal Sensor Connection" figure below
- The sensor for **CPU2** is accessed by **Bits 1-5** of the "Digital I/O ASIC (Port E2h)." Connection of the thermal sensor for **CPU2** is shown in the "CPU2 Thermal Sensor Connection" figure below.

The sensors are based on the Dallas Semiconductor™ DS1620 Digital Thermometer and are located under each processor.



CPU1 Thermal Sensor Connection



CPU2 Thermal Sensor Connection

AIRFLOW REQUIRMENTS

For proper operation, the ZT 5520 must be used in a ventilated environment; however, external forced air is not required.

ADDITIONAL INFORMATION

For more information on programming and reading this device, see the Dallas Semiconductor *DS1620 Digital Thermometer and Thermostat* data sheet. The data sheet is available online at:

http://www.dalsemi.com/DocControl/PDFs/1620.pdf

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

16. FLASH MEMORY

The ZT 5520 implements 2, 4, or 8 Mbytes of on-board flash memory. This memory is partitioned into two areas: one for the system BIOS, which occupies 128 Kbytes, and the other for a non-volatile solid-state disk, which occupies the remaining space. The solid-state disk can be accessed at the P: drive and its size is configured using the "BIOS SETUP Utility Screen." This solid state disk can be used to boot DOS and other user programs. Data can also be logged to this drive. However, since it is a flash memory, it has a limited write cycle life (approximately 100,000 cycles).

The flash disk is mapped in the region 0FFF80000-0FFFBFFFFh, a 256 Kbyte block located 512 Kbytes below the top of 4 Gbytes of memory. The system register (see Chapter 11) is used to control write accesses and page to 256 Kbyte portions. Access to the flash disk is transparent to the user and handled by the BIOS and STD.SYS. The flash disk is readable and writable in the same manner as magnetic media; thus, it can be treated similar to a hard disk.

The BIOS portion of the flash memory is mapped as a 128 Kbyte block in lower memory at E0000h to FFFFFh (896 K to 1 Mbyte). To reprogram the BIOS or to update it if it becomes corrupted, use the FLASH.EXE utility available from Ziatech.

See the following topic, "BIOS Recovery," for instructions on reprogramming the BIOS.

BIOS RECOVERY

The ZT 5520 includes a BIOS Recovery Socket (TB4). If the BIOS becomes corrupted, this 32-pin socket accommodates an EPROM programmed with the BIOS allowing the board to boot when powered on. The EPROM can be ordered from Ziatech (part number ZT 95203-463).

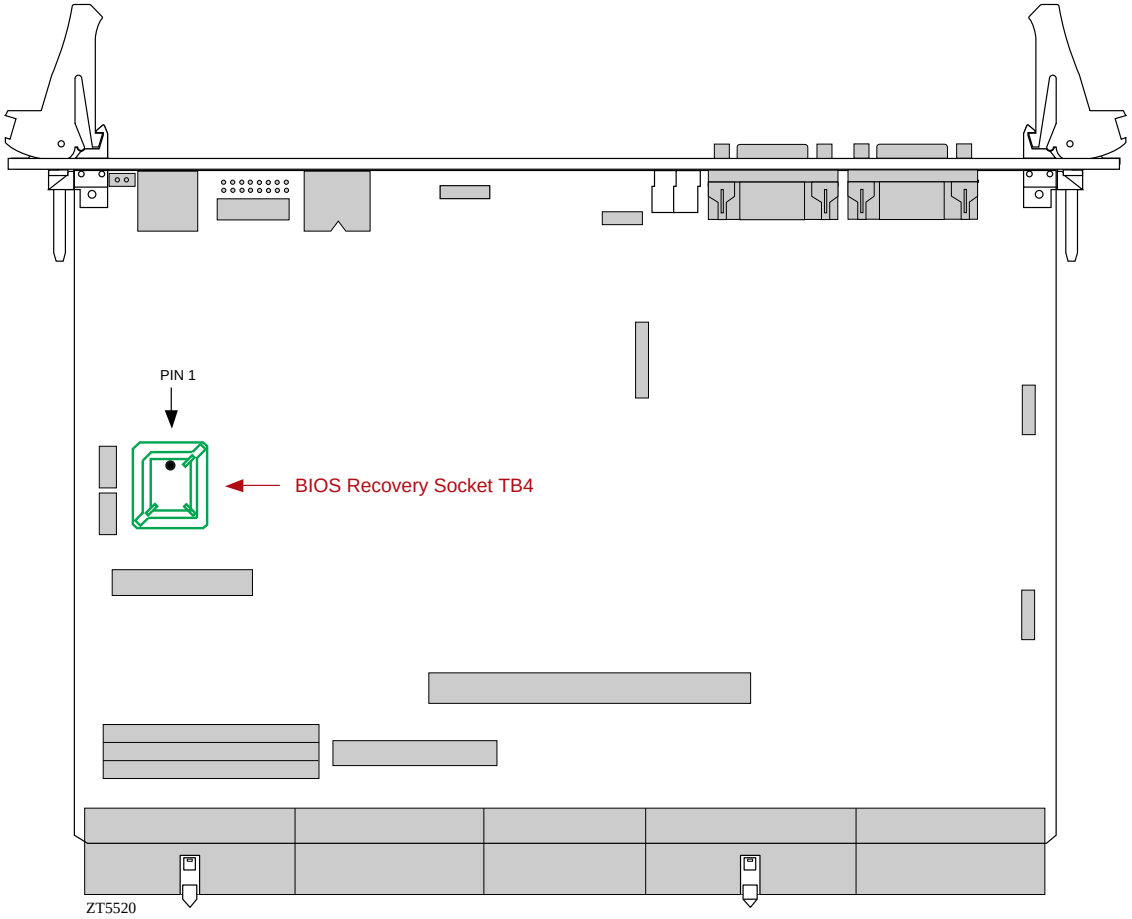
To boot from the boot socket:

1. Close switch SW4-1.

2. Insert the EPROM into the boot socket. Make sure the device is oriented correctly.

3. After powering on the board, reprogram the on-board flash with the BIOS by using the FLASH.EXE utility. Refer to the "Flash Utility Program" section following for detailed instructions.

4. After flashing the BIOS, turn off power, remove the EPROM, and open switch SW4-1.



BIOS Recovery Socket Location

FLASH UTILITY PROGRAM

FLASH.EXE is a utility program that comes on a diskette labeled "Host Development Software Diskette." This diskette is included in all of the Software Development Toolkits Ziatech makes available to support various operating systems. FLASH.EXE allows the user to quickly and conveniently modify the BIOS in the on-board flash memory. This eliminates the need for a PROM programmer and frees the user from having to remove boards and chips from the system. Before attempting to program the flash, make sure that switch SW4-4 is open (Flash Write Protect switch).

To reprogram the BIOS on the ZT 5520, use the following syntax at a DOS prompt:

```
FLASH  /b  sys5520.B00
```

where sys5520.B00 is the BIOS image for the ZT 5520. See the *Ziatech Industrial BIOS for CompactPCI and STD 32 Systems* software manual for more information on the flash utility.

17. ENHANCED IDE INTERFACE

This chapter provides an introduction to the ZT 5520's Enhanced IDE interface controller. It covers the ZT 5520's support for remote EIDE disk drives as well as for on-board solid state IDE capability through the optional ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter.

PRODUCT DEFINITION

The ZT 5520's EIDE interface provides two EIDE channels for interfacing with up to four drives. The EIDE interface is incorporated into the Intel PIIX3 (82371SB) chipset, thus it uses the Peripheral Component Interconnect (PCI) bus to give exceptional EIDE performance. The EIDE interface can sustain a maximum transfer rate of 22 Mbytes per second between the EIDE drive buffer and PCI.

DISK DRIVE SUPPORT

The ZT 5520's EIDE interface supports on-board and remote EIDE disks.

For remote disks, the EIDE controller's signals are routed via rear-panel I/O connector J3 to an optional transition board (such as the ZT 4801-A Rear Panel I/O Transition Board or the ZT 5980 System Utility Board) providing connection to the remote disk. Both the primary and secondary channels are available from J3.

For on-board disks, the EIDE controller's signals are routed to connector J17 for use by solid state disk.

Note: The on-board EIDE disk uses the primary EIDE channel. For simultaneous on-board and remote EIDE capability, remote disks must use the secondary channel. This configuration requires third party software. Contact Ziatech for assistance.

FEATURES OF THE ZT 5520 EIDE INTERFACE

- IBM-AT compatible
- 32-bit, 33 MHz, high performance PCI bus interface
- 22 Mbytes/sec maximum EIDE transfer rate
- Supports PIO and Bus Master EIDE
- Primary and Secondary channels for interfacing up to four devices
- Individual software control for each EIDE channel
- Support for optional on-board solid state disk

SYSTEM REQUIREMENTS

The I/O map for the EIDE interface varies according to the mode of operation. The default mode of operation is "compatibility mode," which means that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h and interrupt IRQ15. No memory addresses are used.

SOLID STATE IDE OPTION

The ZT 5520 supports on-board solid state IDE with the ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter option (ordering option M0-M3. Contact Ziatech). The ZT 96061 connects to the ZT 5520's Flash/IDE expansion connector (J17) and is designed to accommodate CompactFlash expansion cards. These cards appear to the system as a hard drive and are automatically supported by most operating systems.

Note: It is not possible to have both the ZT 96061 and a Ziatech PCI mezzanine board (such as the zPM11 SVGA Mezzanine Board) connected to the ZT 5520 at the same time.

The topics listed below are covered in this section.

- ZT 96061 Input Characteristics
- ZT 96061 Connectors
- ZT 96061 Installation and Removal
- CompactFlash Card Installation and Removal

Input Characteristics

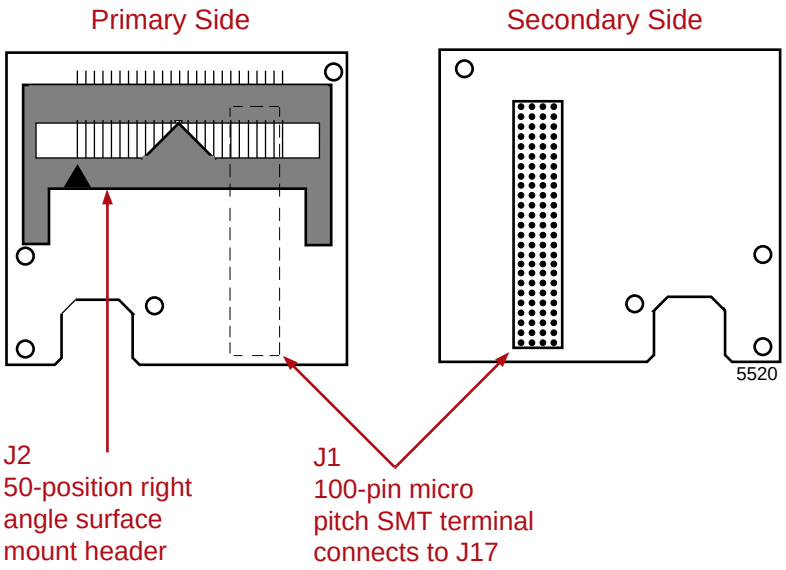
The ZT 96061 works only with Type 1 CompactFlash cards with 3.3 V minimum Vih, I1Z, (Type 1), CMOS voltage input, (Vcc = 5.0 V). SanDisk™ currently manufactures cards with these tolerances.

ZT 96061 Connectors

As shown in the "ZT 96061 Connector Locations" illustration following, the ZT 96061 has two connectors:

J1 A 100-pin male micro pitch terminal for connection to the ZT 5520's flash/IDE expansion connector (J17).

J2 A 50-position right angle surface mount header to interface to CompactFlash expansion cards.



ZT 96061 Connector Locations

ZT 96061 Installation and Removal

The ZT 96061 CompactFlash-to-IDE Mezzanine Adapter plugs into the ZT 5520's flash/IDE expansion connector J17. Mechanical connection is reinforced by metal stand-offs screwed through mounting holes in each PCB.

To install or remove the ZT 96061, perform the steps below.

Installation

1. Put on an anti-static grounding strap.

2. Install the stand-off on the ZT 96061.

3. Correctly orient the ZT 96061 as shown in the "ZT 96061 Orientation" illustration.

4. Align the ZT 96061's J1 connector with connector J17 on the CPU.

5. Applying downward pressure evenly across the length of both connectors, press the ZT 96061 into J17 until the connection is snug.

6. Install the stand-off screw on the back of the CPU.

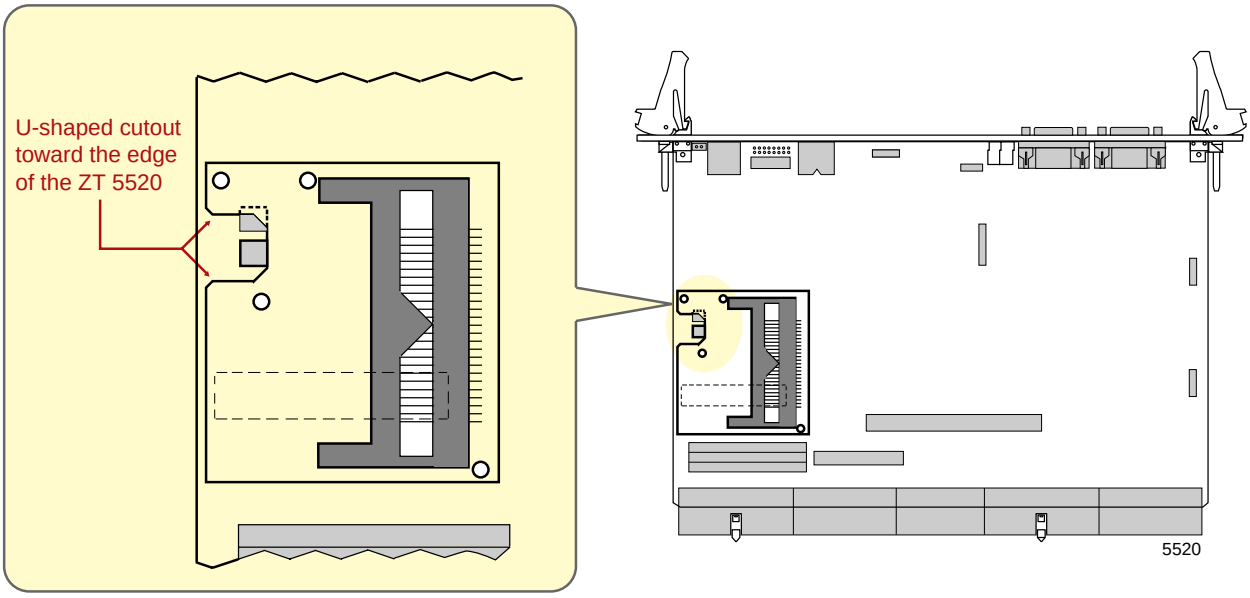
Removal

1. Put on an anti-static grounding strap.

2. Remove the stand-off screws.

3. Using both hands, grasp the edges of the ZT 96061 near the corners and lift gently. While lifting, disengage the pins evenly across the length of the connectors instead of prying only from one side. It may be helpful to gently wiggle the ZT 96061 from front-to-back when removing it.

Warning: To avoid damage to the CPU and the mezzanine card, perform the installation and removal at a static-free workstation.



ZT 96061 Orientation

CompactFlash Card Installation and Removal

To install or remove a CompactFlash card, refer to the "CompactFlash Card Alignment" illustration and perform the steps below.

Installation

1. Make sure the system is powered off.

2. Put on an anti-static grounding strap.

3. Most CompactFlash cards have an arrow on the top label to indicate correct orientation. Align the arrow on the CompactFlash card with the arrow on the surface mount header and slide the card into place until the connection is snug. The dimensions of the grooves in the sides of the CompactFlash card prevent incorrect installation.

Removal

1. Make sure the system is powered off.
2. Put on an anti-static grounding strap.
3. There is a ½ inch U-shaped cutout in the ZT 96061 to assist card removal. Use the cutout area to grasp the card and pull it out of the header.

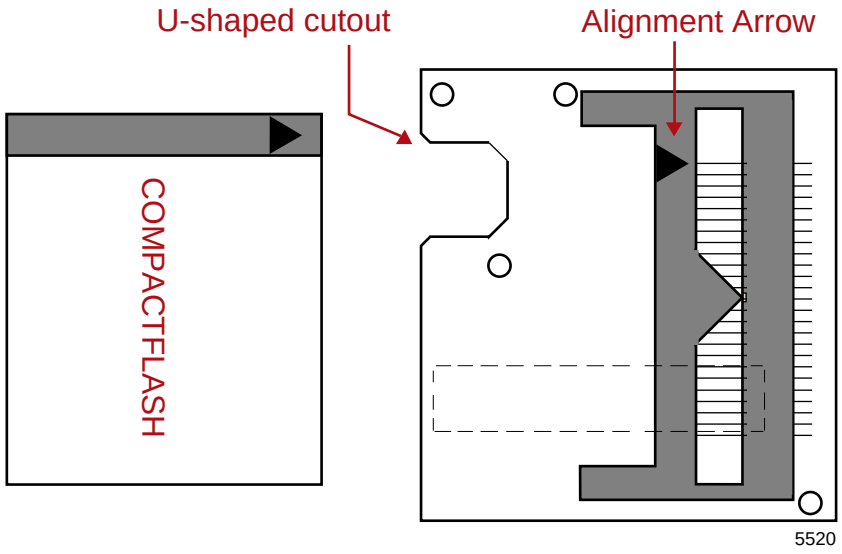
Warning: To avoid damage to the CPU and the mezzanine card, perform the installation and removal at a static-free workstation.

CompactFlash Card Removal

Use the ½ inch U-shaped cutout area to grasp the card and pull it out of the header.

CompactFlash Card Installation

Align the arrow on the CompactFlash card with the arrow on the surface mount header and slide the card into place until the connection is snug. The grooves in the sides of the CompactFlash card prevent incorrect installation.



CompactFlash Card Alignment

DRIVE CONFIGURATION

The ZT 5520's BIOS will automatically configure the drive for you. To configure the EIDE drive, access the BIOS SETUP utility screen by typing the **"S"** key during the boot sequence and select "AUTO" for the drive configuration. The BIOS will query the drive to determine the correct settings. Some external drives may need to be set up manually if the AUTO configuration does not work. Consult your drive manual for details on the disk geometry should this be the case.

Note: The on-board EIDE disk uses the primary EIDE channel. For simultaneous on-board and off-board EIDE capability, off-board disks must use the secondary channel. This configuration requires third party software. Contact Ziatech for assistance.

See the section "Setup" in Chapter 2 for more on the BIOS setup.

DEVICE DRIVERS

The EIDE interface works with all applications by default. To fully utilize the EIDE interface, you may install additional drivers to increase the performance under MS-DOS, Windows 3.X, Windows 95, Windows NT, IBM® OS/2®, SCO®, UNIX, and Novell® Netware™. Contact the vendors of individual operating systems for the latest drivers for the Intel PIIX3 (82371SB) EIDE interface.

Note: You may have difficulty installing the QNX operating system, ver. 4.24, on CompactFlash cards. If problems occur, restart the install program and specify regular IDE drivers (Fsys.ide) instead of the default EIDE drivers (Fsys.eide).

ADDITIONAL INFORMATION

Refer to the Intel *82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator* data sheet for more information on the PIIX3 Reset Control register. The data sheet is available online at:

http://developer.intel.com/design/chipsets/datashts/290550.htm

The data sheet is in Adobe Acrobat format (PDF). If you do not have the Acrobat Reader, it is available on the Adobe Home Page at http://www.adobe.com.

For more information about CompactFlash and the *CompactFlash Specification*, visit the CompactFlash Association website:

http://www.compactflash.org.

A. BOARD CONFIGURATION

The ZT 5520 includes several options that tailor the operation of the board to requirements of specific applications. Most of the options are selected through the BIOS SETUP mechanism. Some options cannot be software controlled and are configured with switches or cuttable traces. Switch options are made by closing or opening the desired switch. Cuttable trace options are made by installing and removing surface mount zero ohm (0603 size) resistors.

This appendix covers switch and cuttable trace options. It also provides illustrations showing the locations of switches and cuttable traces on the ZT 5520.

BIOS SETUP OPTIONS

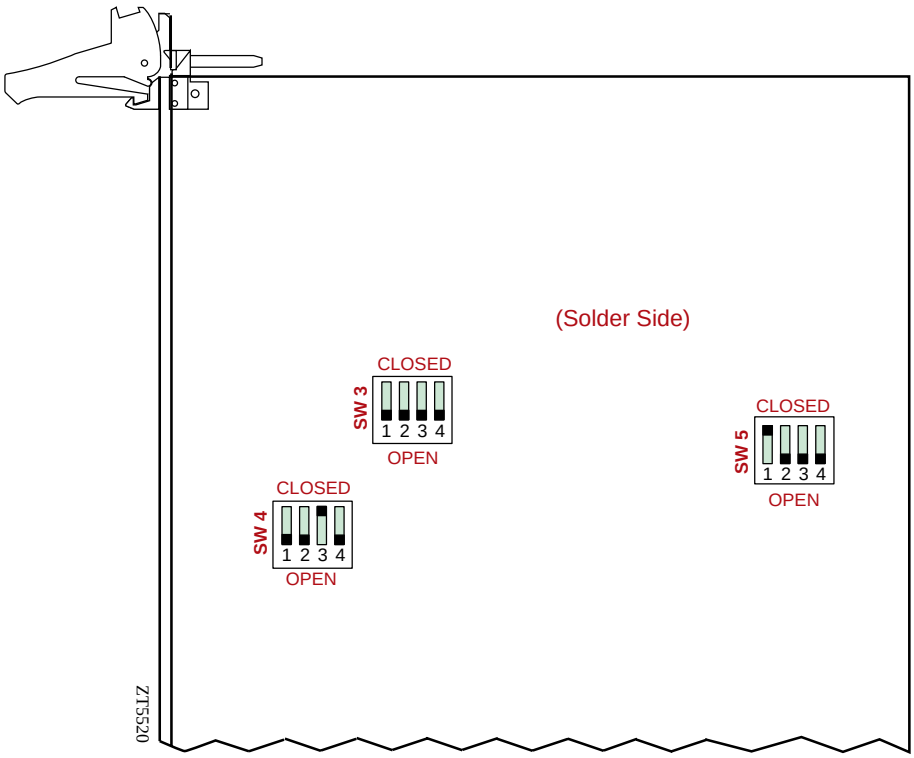
The ZT 5520 has several features that can be configured with the BIOS SETUP program. The SETUP program is executed during the boot sequence when the "**S**" key is typed. In DOS systems, SETUP may also be executed by running the SETUP.COM program from the DOS command line.

For setup procedures and configuration of the ZT 5520, as well as for an illustration of the BIOS SETUP utility screen, see the section "Setup" in Chapter 2.

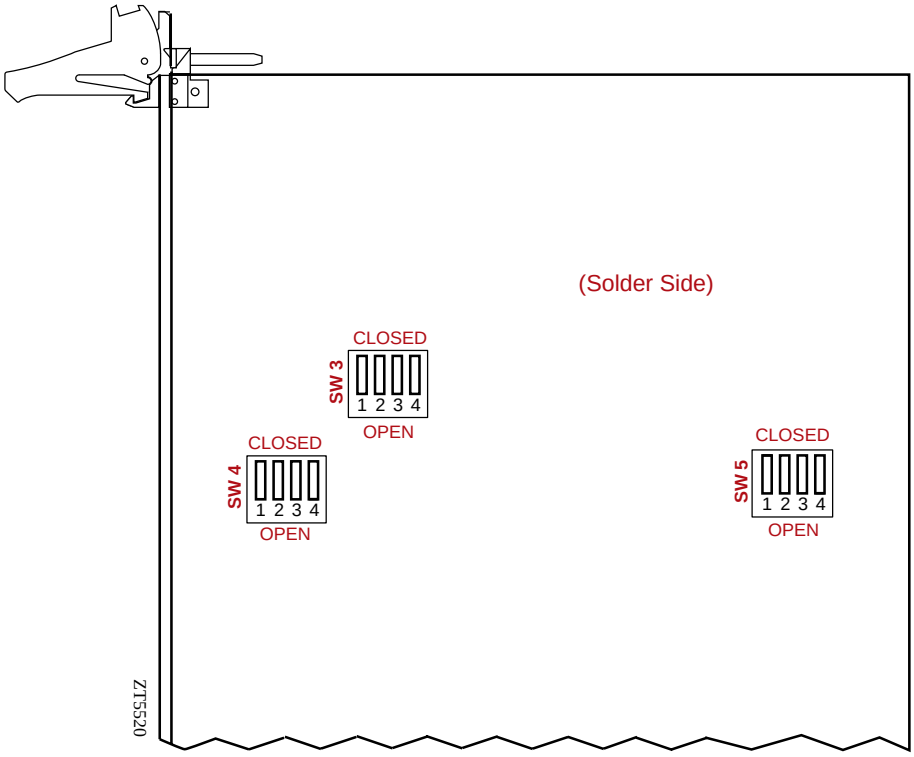
SWITCH OPTIONS AND LOCATIONS

The ZT 5520 contains three banks of switches located on the solder side of the board. SW1 and SW2 are push-button switches located on the front panel of the board.

The "Factory Default Switch Configuration" figure illustrates the factory default switch settings for ZT 5520 boards purchased in a DOS system. The following illustration "Customer Switch Configuration" provides a blank switch layout; use this figure to document your switch configuration if it differs from the factory default.



Factory Default Switch Configuration



Customer Switch Configuration

SWITCH CROSS-REFERENCE TABLE

The "Switch Cross-Reference" table divides the switch options into functional groups.

Switch Cross Reference

Function	Switch
Abort - NMI Generation	SW1 (push-button on front panel)
BIOS Recovery	SW4-1
CMOS Clear / Battery Backup	SW5-1, SW5-2
Flash Write Protect	SW4-4
ISA Bus Speed	SW4-3
JTAG Daisy Chain	SW5-4
Reserved	SW5-3
Port 80 Test Mode	SW4-2
Reset	SW2 (push-button on front panel)
Software Configuration	SW3-1, SW3-2, SW3-3, SW3-4

SWITCH DESCRIPTIONS

The following topics list the switches in numerical order and provide a detailed description of each switch. A dagger (†) indicates the default switch configuration.

Note that where switches are referenced in this chapter, "SWx" corresponds to the switch number and "-N" corresponds to the switch position (for example, SW4-2 means "switch number 4, position 2"). A switch referred to as "closed" is also considered "on."

SW1 (Abort - NMI Generation)

This switch, when pressed, will issue an ABORT (NMI) to the processor. SW1 is a push-button on the ZT 5520's front panel.

SW2 (Reset)

This switch, when pressed, will issue a hard reset to the board. SW2 is a push-button on the ZT 5520's front panel.

SW3-1, SW3-2, SW3-3, SW3-4 (Software Configuration)

These switches can be monitored by the user's software through the Digital I/O ASIC (PortE4h) to provide user configurable features (see Chapter 11, "System Registers"). When open, these switches read back a "0" and when closed read back a "1". Factory default is open.

SW3-1, -2, -3, -4

State	Read-back
† Open	0
Closed	1

SW4-1 (BIOS Recovery)

This switch is used to boot from the BIOS Recovery Socket (TB4). When SW4-1 is open, the BIOS boots from the on-board flash memory. When SW4-1 is closed, the BIOS boots from the BIOS Recovery Socket (TB4). See the section, "BIOS Recovery," in Chapter 16 for more information. Factory default is open.

SW4-1	Function
† Open	Normal operation
Closed	Boot from the BIOS recovery socket (TB4)

† Factory default configuration

SW4-2 (Port 80 Test Mode)

This switch sets the Digital I/O ASIC (Port E0h) to decode accesses to I/O port 80h in addition to E0h. The system BIOS outputs Port 80 POST codes during bootup. The Port 80 data is output on Port 0, bits 0 to 7. These bits can be accessed at the flash/IDE expansion connector J17. Use this mode for debugging custom software and hardware. The Digital I/O ASIC (Port E0h) is also accessible at its default address (E0h). The status of SW4-2 can be read back at Digital I/O ASIC (Port E4h), bit 6. Factory default is open.

SW4-2	Function
† Open	Normal operation
Closed	Port 80h Test Mode

SW4-3 (ISA Bus Speed)

This switch is used to select the speed of the on-board internal ISA bus. For 30 and 33 MHz bus speeds, this switch should be closed (7.5 MHz and 8.25 MHz ISA bus speeds, respectively). The status of this switch can be read back at Digital I/O ASIC (Port E4h), bit 5.

Factory default for SW4-3 is closed.

SW4-3	Function
† Closed	PCI bus speed ÷ 4

SW4-4 (Flash Write Protect)

Closing this switch write protects the BIOS and flash disk portion of the flash memory. This switch must be open when using the FLASH.EXE utility to recover from a corrupted BIOS. The status of this switch can be read back at Digital I/O ASIC (Port E4h), bit 4. Factory default is open.

SW4-4	Function
† Open	flash Disk/BIOS read/write
Closed	flash Disk/BIOS read only

† Factory Default Configuration

SW5-1, SW5-2 (CMOS Clear / Battery Backup)

These switches are used to battery back and clear the CMOS memory. When closed, SW5-1 connects the CMOS memory to the on-board battery. For normal operation this switch should remain in the closed position. If for some reason the CMOS needs to be cleared, open SW5-1 and close SW5-2 to clear the CMOS. After the CMOS has been cleared, return SW5-2 to the open position and SW5-1 to the closed position. Factory default is SW5-1 closed and SW5-2 open.

Note: Do not have SW5-1 and SW5-2 closed at the same time.

	SW5-1	SW5-2	CMOS Configuration RAM
†	Closed	Open	Normal operation - battery backed
	Open	Closed	Clear CMOS (return to default after clearing)

SW5-3 (Reserved)

This switch is reserved for future use.

SW5-4 (JTAG Daisy Chain)

This switch, when closed, connects the JTAG signals TDI to TDO at the CompactPCI mezzanine connector J18. This allows completion of the JTAG chain without having a peripheral in the mezzanine connector. Factory default is open.

	SW5-4	Function
†	Open	TDI/TDO unconnected
	Closed	TDI/TDO connected

CUTTABLE TRACE OPTIONS AND LOCATIONS

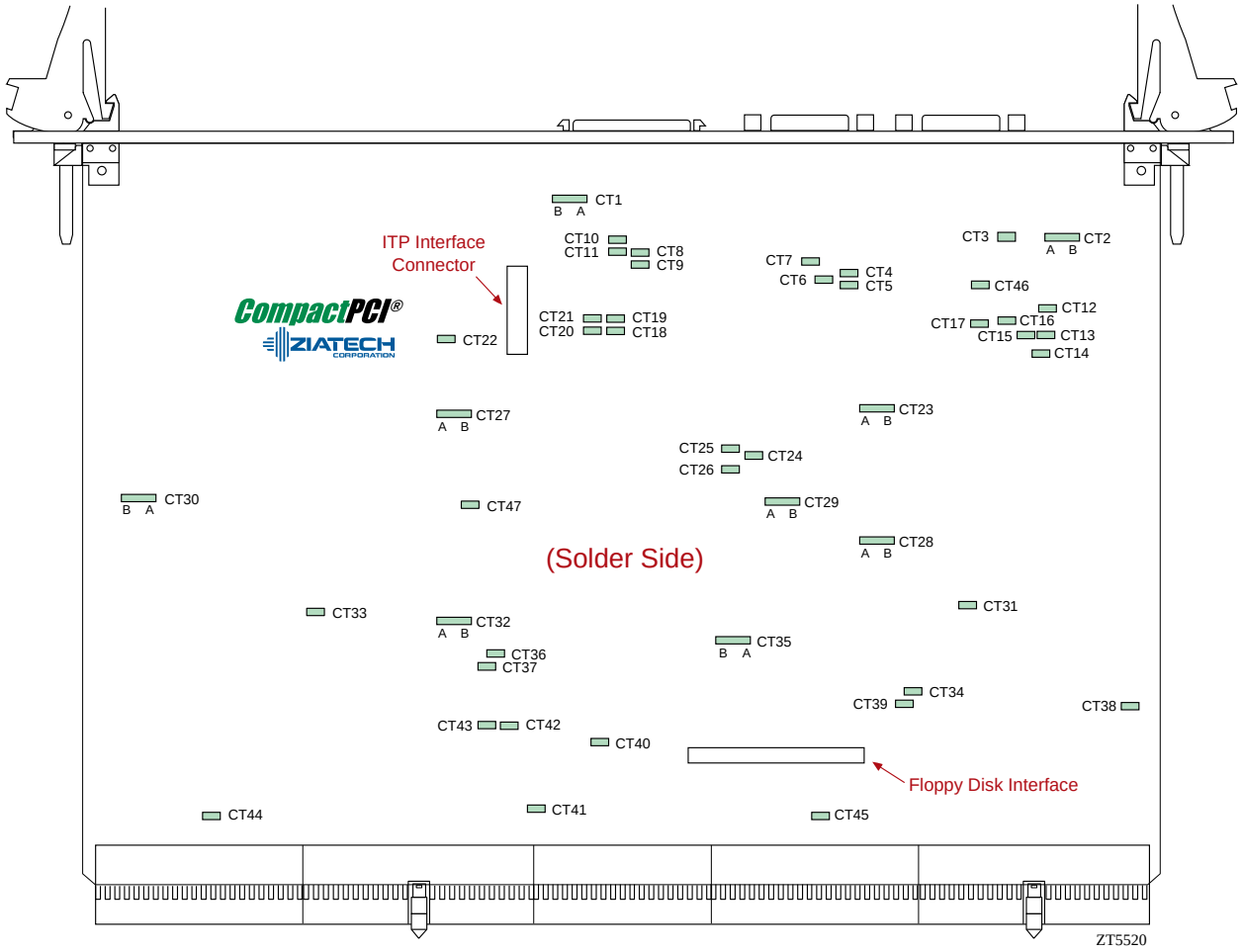
The ZT 5520 contains several cuttable traces (zero ohm shorting resistors) that allow the user to configure other board options. The "Cuttable Trace Locations" figure shows the placement of the ZT 5520 cuttable traces. The "Cuttable Trace Definitions" table provides a quick cross-reference for the ZT 5520 cuttable trace descriptions that follow.

There are two types of cuttable traces on the ZT 5520: single-option and double-option. **Single option cuttable traces** are implemented using 0603 surface mount pads. A zero ohm shorting resistor is then soldered between these pads to make the

† Factory Default Configuration

connection. **Double option cuttable traces** (CT1, CT2, CT23, CT27, CT28, CT29, CT30, CT32, CT35) are implemented using three 0603 surface mount pads. The zero ohm shorting resistor is then soldered between one set of pads, depending on the chosen option.

Note: Cuttable trace modifications should only be performed by a qualified technician familiar with surface mount soldering techniques. The product warranty is voided if the board is damaged by customer modifications. If a qualified technician is not available to you, contact Ziatech Technical Support. For large production orders Ziatech can also set up "specials" that are pre-configured at the factory. Contact Ziatech for more information.



Cuttable Trace Locations

Cuttable Trace Definitions

CT#	DEFAULT	DESCRIPTION
CT1	B	12V VRM fan (A for 5V fan)
CT2	B	3.3 V Voltage Monitor (A for 5V)
CT3	IN	Enable Backplane Reset from J1/J2
CT4	IN	Board Revision
CT5	IN	Board Revision
CT6	IN	Board Revision **(no load w/ CT47 in)**
CT7	IN	Board Revision
CT8	OUT	VccP2 test bit 0
CT9	OUT	VccP2 test bit 1
CT10	OUT	VccP2 test bit 2
CT11	OUT	VccP2 test bit 3
CT12	OUT	CPU core frequency configuration bit 1
CT13	IN	CPU core frequency configuration bit 0
CT14	IN	Part 1210 (out for 1312)
CT15	IN	CPU core frequency configuration bit 3
CT16	IN	CPU core frequency configuration bit 2
CT17	IN	PIIX3 USB clock enable
CT18	OUT	VccP1 test bit 0
CT19	OUT	VccP1 test bit 1
CT20	OUT	VccP1 test bit 2
CT21	OUT	VccP1 test bit 3
CT22	IN	CPU2 THERMTRIP# to E1h bit 7
CT23	A	5V Vpp for flash 2 (BD4) (B for 12V)
CT24	IN	SMI# signals ECC error to CPU
CT25	IN	CPU bus frequency configuration
CT26	OUT	CPU bus frequency configuration

Cuttable Trace Definitions (con'd)

CT#	DEFAULT	DESCRIPTION
CT27	A	Dual P6 JTAG enable (B for CPU1 only)
CT28	A	5V Vpp for flash 1 (BD6) (B for 12V)
CT29	B	APIC SMI# (A for PIIX3 SMI#)
CT30	B	12 V CPU fans (A for 5 V fans)
CT31	OUT	J1/J2 Bridge configuration straping
CT32	A	Dual P6 JTAG enable (B for CPU2 only)
CT33	IN	CPU1 THERMTRIP# to E1h bit 6
CT34	OUT	Disable INTP from J18 to IRQ14
CT35	A	DRAM OE# control (B for OE)
CT36	OUT	Disable clock synth feedback bypass
CT37	OUT	Disable clock synth feedback bypass
CT38	OUT	Disable J1/J2 JTAG data loop
CT39	OUT	Disable INTS from J18 to IRQ15
CT40	OUT	J4/J5 Bridge config straping
CT41	OUT	Disable J4/J5 JTAG data loop
CT42	IN	Clock synth frequency select
CT43	OUT	Clock synth frequency select
CT44	IN	Enable Backplane Reset from J4/J5
CT45	OUT	Floppy drive configuration
CT46	OUT	Configuration logic voltage monitor
CT47	OUT	CPUPRES2# route to ASIC E3h bit 4

CT1, CT30 (Fan Connector Voltage)

These cuttable traces allow for use of a 5 V or 12 V fan. VRM cooling is available through connector J11. CPU cooling is available through connectors J16 and J20.

VRM Cooling

CT1	A	5 V
	† B	12 V

CPU Cooling

CT30	A	5 V
	† B	12 V

CT2 (Voltage Monitor Setting)

This cuttable trace is reserved for factory use only.

CT3, CT44 (Backplane Reset)

When installed, these cuttable traces enable resets from the backplane to reset the ZT 5520, according to the following table.

	CT3	Function
†	IN	Reset enabled from the CompactPCI bus to connectors J1/J2
	OUT	Reset disabled from the CompactPCI bus to connectors J1/J2

	CT44	Function
†	IN	Reset enabled from the CompactPCI bus to connectors J4/J5
	OUT	Reset disabled from the CompactPCI bus to connectors J4/J5

† Factory Default Configuration

CT4-CT7 (Board Revision)

These cuttable traces are set at the factory depending on the current board revision and should not be modified by the user.

Note: CT6 should not be loaded if CT47 is installed.

CT8-CT11, CT18-CT21 (CPU Core Voltage Test)

These cuttable traces are reserved for factory use only. ***Loading these cuttable traces could damage the processors.***

CT12-13, CT15-16, CT25-26, CT42-43 (CPU Bus Frequency/Core Factor)

These cuttable traces are used to control the CPU/PCI bus frequency and CPU Speed Multiplier for different speed processors as shown in the following table.

Speed (MHz)			Cuttable Traces							
CPU Core	CPU Bus	PCI Bus	CT 12	CT 13	CT 15	CT 16	CT 25	CT 26	CT 42	CT 43
200	66.7	33.3	OUT	IN	IN	IN	IN	OUT	IN	OUT

Bus Frequency Settings

CT25, CT26, CT42 and CT43 are used to set the CPU and PCI bus frequency. The PCI bus frequency is always one-half of the CPU bus frequency.

Speed (MHz)		Cuttable Traces			
CPU Bus	PCI Bus	CT25	CT26	CT42	CT43
60	30	OUT	IN	OUT	IN
66.7	33.3	IN	OUT	IN	OUT

CPU Speed Multiplier Settings[‡]

CT12, CT13, CT15, and CT16 are used to set the multiplication factor of the internal CPU clock.

Core/Bus	Cuttable Traces			
	CT12	**CT13**	**CT15**	**CT16**
2X	IN	IN	IN	IN
2.5X	IN	OUT	IN	IN
3X	OUT	IN	IN	IN
3.5X	OUT	OUT	IN	IN
4X	IN	IN	IN	OUT

CT14 (Part 1210/1312)

This cuttable trace is reserved for factory use only.

CT17 (PIIX3 USB Clock)

Removing this cuttable trace disables the clock signal to the USB controller contained within the PIIX3 (TD4) device. Factory default configuration is in.

[‡] A.CPUSpeedMultiplierSettings

CT22, CT33 (CPU THERMTRIP# Enable)

Installing CT22 and CT33 allows the CPU THERMTRIP# signal to be monitored at Digital I/O ASIC (Port E1h). If the processor core exceeds 130°C and the processor halts, the THERMTRIP# signal is driven active from each CPU to a bit in Digital I/O ASIC (Port E1h), according to the following table.

Cuttable Trace	Position	Signal Routing
CT22	† IN	CPU2 (TN3) THERMTRIP# to E1h bit **7**
	OUT	Signal not monitored
CT33	† IN	CPU1 (TN7) THERMTRIP# to E1h bit **6**
	OUT	Signal not monitored

CT23, CT28 (Flash Voltage)

These cuttable traces are reserved for factory use only.

CT24 (SMI# Routing)

Installing CT24 allows single bit ECC errors to be reported to the CPU via the SMI# signal generated from the PIIX3 (TD4) device.

CT27, CT32 (CPU JTAG Routing)

These cuttable traces allow JTAG data to bypass an empty CPU socket. When JTAG testing is required, the cuttable traces should be loaded according to the following table.

	Loaded CPU	CT27	CT32
†	Both	A	A
	CPU1 only	B	A
	CPU2 only	A	B

† Factory Default Configuration

CT29 (SMI# Routing)

Installing CT29 selects the SMI# signal routing from the PIIX3 (TD4) device, according to the following table.

Position	SMI# Signal Routing
A	Through the I/O APIC (TD5) device for redirection by software to either the APIC bus or the CPU SMI#.
B	I/O APIC bypassed; signal routed directly to CPU.

CT31, CT40 (PCI Bridge Configuration)

These cuttable traces are reserved for factory use only.

CT34 (INTP- Support)

Installing CT34 enables the INTP- signal on the mezzanine connector (J18). Factory default configuration for CT32 is out.

CT35 (DRAM OE# Control)

This cuttable trace is reserved for factory use only.

CT36, CT37 (Clock Synth Feedback)

This cuttable trace is reserved for factory use only.

CT38, CT41 (Backplane JTAG)

When installed, these cuttable traces connect backplane JTAG signals TDI and TDO on CompactPCI connectors J1, J2 and J4, J5, according to the following table.

	CT38	Function
	IN	TDI/TDO connected on J1/J2
†	OUT	TDI/TDO not connected on J1/J2

	CT41	Function
	IN	TDI/TDO connected on J4/J5
†	OUT	TDI/TDO not connected on J4/J5

CT39 (INTS- Support)

CT39 enables the INTS- signal on the mezzanine connector (J18).

CT45 (Floppy Drive Configuration)

This cuttable trace is reserved for factory use only.

CT46 (Configuration Logic Voltage Monitor)

This cuttable trace is reserved for factory use only.

CT47 (CPU PRES2# Routing)

This cuttable trace is reserved for factory use only.

Note: CT6 should not be loaded if CT47 is installed.

† Factory Default Configuration

B. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 5520. It includes illustrations of the board dimensions and connector locations, connector pinout tables, and example schematics showing connection of various peripherals to the rear-panel user I/O connector.

ELECTRICAL AND ENVIRONMENTAL

The following topics provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- DC/DC voltage settings
- Battery backup characteristics

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 5520 at these maximums. See the "DC Operating Characteristics" section in this appendix for operating conditions.

- Supply Voltage, Vcc: 0 to 5.5 V
- Supply Voltage, AUX +: 0 to 12.6 V (required for 8 Mbyte and 4 Mbyte flash programming and fan/heatsinks only; 2 Mbyte flash operation does not require +12 V)
- Supply Voltage, AUX -: Not used
- Storage Temperature: -40° to +85° Celsius
- Non-Condensing Relative Humidity: <95% at 40º Celsius

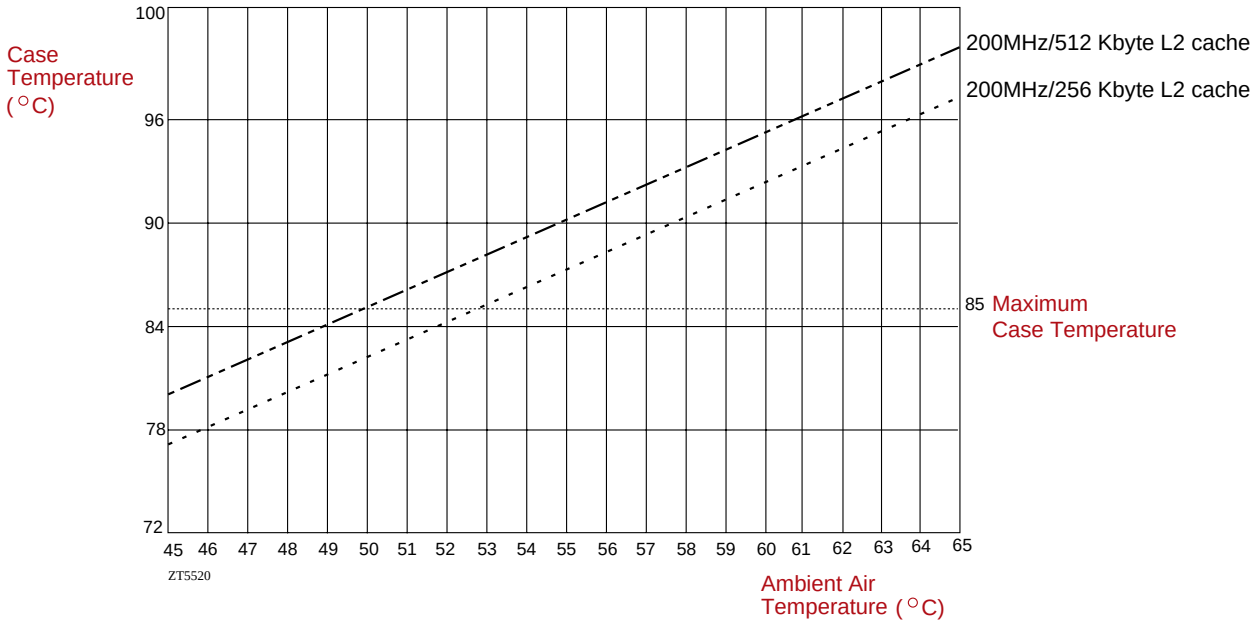
Operating Temperature

For proper operation of the ZT 5520, the Pentium Pro processor case temperature must remain below 85° Celsius. An integrated fan/heatsink is provided with the processor to help maintain this requirement. See the "Pentium Pro Processor Maximum Ambient Temperature" table below.

Pentium Pro Processor Maximum Ambient Temperatures

Processor Speed (MHz/Kbytes L2)	Max. Ambient Temperature (°C)
200/256	52.8
200/512	50.0

The figure below "Ambient Temperature Vs. Pentium Pro Processor Case Temperature" shows the **relationship** between ambient temperature and case temperature (when operated with the integrated fan/heatsink) for the processor sold with the ZT 5520.



Ambient Temperature Vs. Pentium Pro Processor Case Temperature

DC Operating Characteristics

- Supply Voltage, Vcc: 4.8 to 5.25 V
- Supply Voltage, AUX +: 11.4 to 12.6 V
- Supply Voltage, AUX -: Not used
- Supply Current, Icc:
- Processor option/cache size specifications

Processor Option	Option	Icc typ(A)	Icc max(A)
Single 200 MHz			
256Kbyte L2		6.2	9.7
512Kbyte L2	2C1	11.1	16.0
Dual 200 MHz			
256Kbyte L2	1C2	7.5	11.0
512Kbyte L2	2C2	13.2	18.0

(Numbers assume 32 Mbytes of DRAM and 2 Mbytes of flash. Each additional 32 Mbytes adds 0.4 A typ., 0.8 A max.)

- Supply Current, AUX + (12 V):

--4 Mbyte flash Option: 0.010 A typ., 0.015 A max.

--8 Mbyte flash Option: 0.020 A typ., 0.030 A max.

--Single Fan/Heatsink: 150 mA typ., 200 mA max.

--Dual Fan/Heatsink: 300 mA typ., 400 mA max.

DC/DC Voltage Settings

The ZT 5520 contains four DC/DC converters. Each Pentium Pro processor is supported by a converter which is self-configured for the processor's required core voltage. Another converter is used for the processor's L2 cache and other 3.3 V devices (i.e., DRAM, chipset). The final converter is used to drive the CPU (GTL+) bus. The board is configured from the factory to the correct voltage for the loaded processor(s).

Battery Backup Characteristics

- Battery Voltage: 3 V
- Battery Capacity: 255 mAH
- Real-Time Clock Requirements: 4 µA max. (Vbat = 3 V, Vcc=0 V)
- Real-time clock data retention:

  --56250 Hours/ 6.4 years min. (in the absence of power)

  --9.6 years min. (with Vcc power applied 8 hours per day)

- Electrochemical Construction: Poly-carbonmonofluoride

MECHANICAL

This section includes the following mechanical specifications:

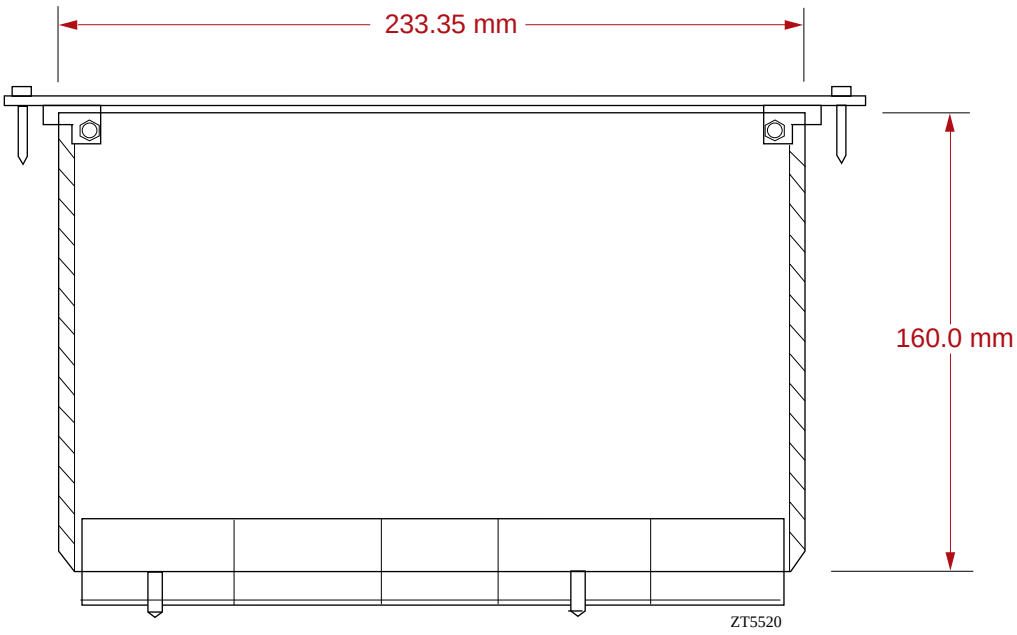
- Card dimensions and weight
- Connectors (including connector locations, descriptions, and pinouts)
- Example schematics showing connection of standard peripherals to the rear-panel user I/O connector

Card Dimensions and Weight

The ZT 5520 is compliant with the *CompactPCI Specification, PICMG 2.0, Version 2.1* for all mechanical parameters. In a CompactPCI enclosure with 0.8 inch spacing, the ZT 5520 requires two card slots with the integrated fan/heatsink.

Mechanical dimensions are shown in the "Board Dimensions" illustration and are outlined below.

- Board Length: 160 mm
- Board Width: 233.35 mm
- Board Thickness: 1.6 mm (0.063 inches)
- Board Weight: 822 grams (29 ounces) with heatsink/fan



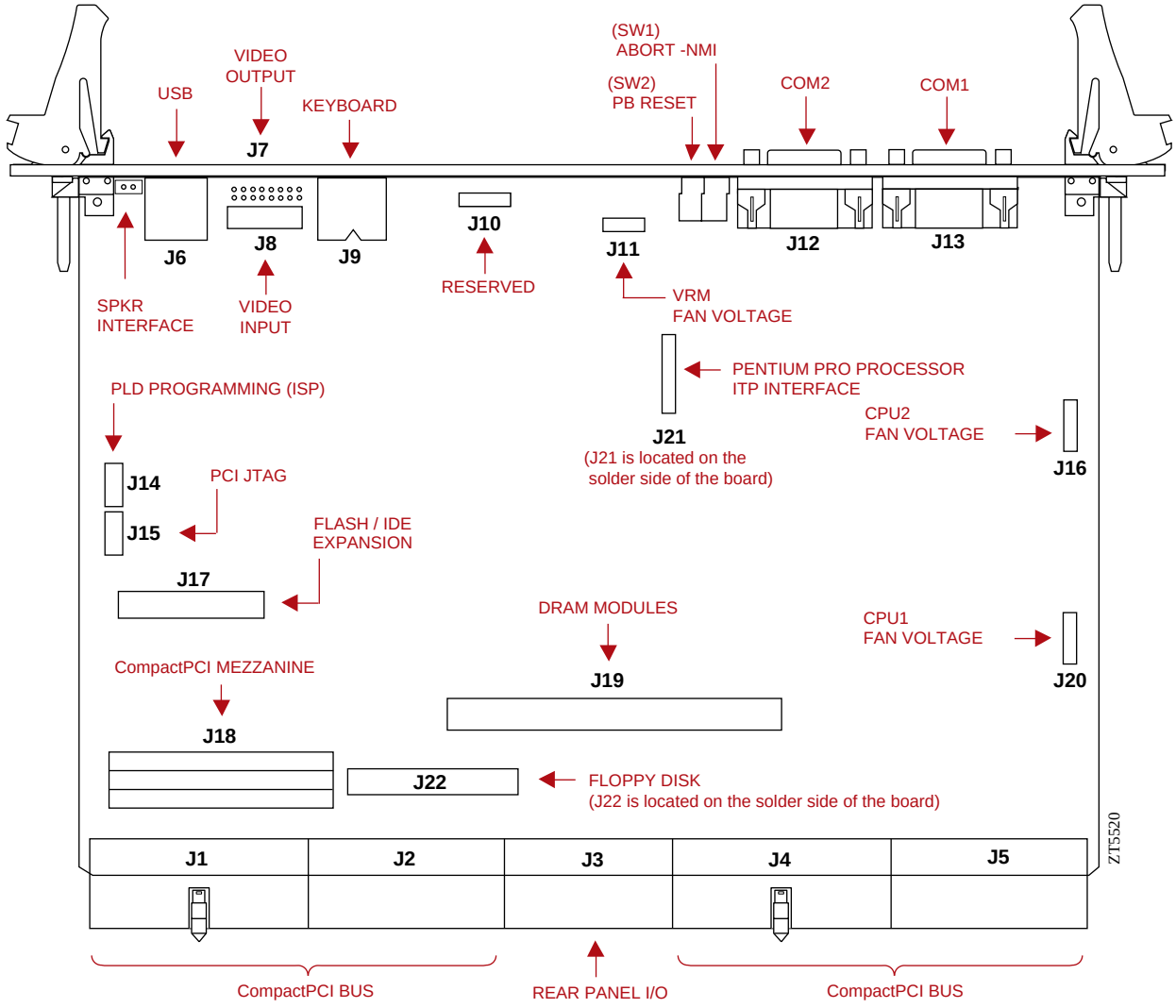
Board Dimensions

Connectors

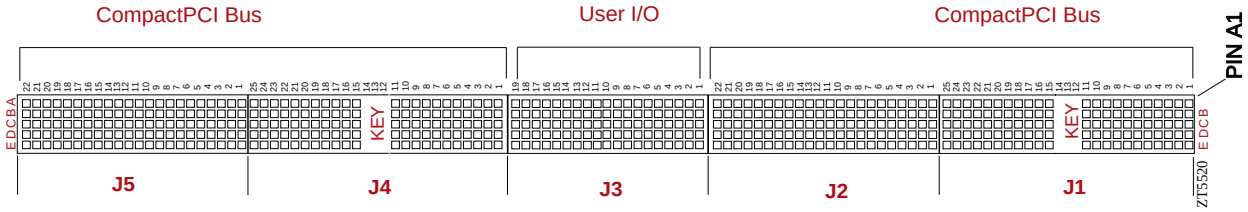
As shown in the "Connector Locations" figure, the ZT 5520 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table below. A description and pinout for each connector is given in the following topics.

Connector Assignments

J1, J4	CompactPCI Bus Connectors
J2, J5	CompactPCI Bus Connectors
J3	Rear-Panel User I/O Connector
J6	Universal Serial Bus Interface Connector
J7, J8	Video Output/Input Connectors
J9	Keyboard Interface Connector
J10	Reserved
J11, J16, J20	Fan Power Connectors
J14	PLD Programming Interface Connector
J15	General JTAG Interface Connector
J17	Flash/IDE Expansion Connector
J18	Mezzanine PCI Interface Connector
J19	DRAM Interface Connector
J21	Pentium Pro ITP Interface Connector
J22	Floppy Disk Drive Interface Connector



Connector Locations



CompactPCI Connector Pin Locations

J1, J4 (CompactPCI Bus Connectors)

J1 and J4 are 110-pin 2 mm x 2 mm right-angle female connectors. See the "J1, J4 CompactPCI Interface Connector Pinout" table below for pin definitions and the "CompactPCI Connector Pin Locations" figure above showing pin placement.

J1, J4 CompactPCI Interface Connector Pinout

Pin#	A	B	C	D	E	F
25	5V	REQ64#	BRSV	3.3V	5V	GND (Shield)
24	AD[1]	5V	V(I/O)(2)	AD[0]	ACK64#	GND (Shield)
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND (Shield)
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND (Shield)
21	3.3V	AD[9]	AD[8]	M66EN(5)	C/BE[0]#	GND (Shield)
20	AD[12]	GND	V(I/O)(2)	AD[11]	AD[10]	GND (Shield)
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND (Shield)
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND (Shield)
17	3.3V	SDONE	SBO#	GND	PERR#	GND (Shield)
16	DEVSEL#	GND	V(I/O)(2),(6)	STOP#	LOCK#	GND (Shield)
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND (Shield)
14						
13			KEY AREA			
12						
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND (Shield)
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND (Shield)
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND (Shield)
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND (Shield)
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND (Shield)
6	REQ#	GND	3.3V	CLK	AD[31]	GND (Shield)
5	BRSVP1A5(12)	BRSVP1B5(12)	RST#	GND	GNT#	GND (Shield)
4	BRSVP1A4(12)	GND	V(I/O)	NC	NC	GND (Shield)
3	INTA#	INTB#	INTC#	5V	INTD#	GND (Shield)
2	TCK	5V	TMS	TDO	TDI	GND (Shield)
1	5V	-12V	TRST#	+12V	5V	GND (Shield)
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

J2, J5 (CompactPCI Bus Connectors)

J2 and J5 are 110-pin 2 mm x 2 mm right-angle female connectors. See the "J2, J5 CompactPCI Interface Connector Pinout" table below for pin definitions and the "CompactPCI Connector Pin Locations" figure showing pin placement.

J2, J5 CompactPCI Interface Connector Pinout

Pin#	A	B	C	D	E	F
22	NC	NC	NC	NC	NC	GND (Shield)
21	NC	NC	NC	NC	NC	GND (Shield)
20	NC	NC	NC	NC	NC	GND (Shield)
19	NC	NC	NC	NC	NC	GND (Shield)
18	NC	NC	NC	NC	NC	GND (Shield)
17	NC	GND	PRST#	REQ#6	GNT6#	GND (Shield)
16	NC	NC	DEG#	GND	NC	GND (Shield)
15	NC	GND	FAL#	REQ#5	GNT5#	GND (Shield)
14	NC	NC	NC	NC	NC	GND (Shield)
13	NC	NC	NC	NC	NC	GND (Shield)
12	NC	NC	NC	NC	NC	GND (Shield)
11	NC	NC	NC	NC	NC	GND (Shield)
10	NC	NC	NC	NC	NC	GND (Shield)
9	NC	NC	NC	NC	NC	GND (Shield)
8	NC	NC	NC	NC	NC	GND (Shield)
7	NC	NC	NC	NC	NC	GND (Shield)
6	NC	NC	NC	NC	NC	GND (Shield)
5	NC	NC	NC	NC	NC	GND (Shield)
4	NC	NC	NC	NC	NC	GND (Shield)
3	CLK4	GND	GNT3#	REQ#4	GNT4#	GND (Shield)
2	CLK2	CLK3	GND	GNT2#	REQ#3	GND (Shield)
1	CLK1	GND	REQ#1	GNT1#	REQ#2	GND (Shield)
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

J3 (Rear-Panel User I/O Connector)

J3 is a 95-pin 2 mm x 2 mm female connector providing rear-panel user I/O. See the following table "J3 Rear-Panel User I/O Connector Pinout" for pin definitions and the "CompactPCI Connector Pin Locations" figure showing pin placement. The signals shown in the pinout table are specific to the ZT 5520 implementation and are used by the ZT 5980 System Utility Board to provide access to various I/O peripherals through standard connector configurations.

For example schematics showing connection of various peripherals to connector J3, see the section, "Schematics: Rear-Panel User I/O Connection," at the end of this appendix.

The following I/O peripherals are available on this connector:

• COM1	• USB
• COM2	• Keyboard
• LPT	• PS/2 Mouse
• Floppy	• IDE primary and secondary channels

J3 Rear-Panel User I/O Connector Pinout

Pin#	A	B	C	D	E	F
19	PWRGD	ISAIO16-	IORDY	MIRQ0	IRQ14	GND (Shield)
18	CS3S-	CSIS-	CS3P-	CS1P-	DDAK1-	GND (Shield)
17	DD15	DD14	DD13	DD12	DDRQ1	GND (Shield)
16	DD11	DD10	DD9	DD8	DDAK0-	GND (Shield)
15	DA0	DA1	VCC	DA2	DDRQ0	GND (Shield)
14	DD7	DD6	DD5	DD4	DIOW-	GND (Shield)
13	DD3	DD2	DD1	DD0	DIOR-	GND (Shield)
12	DRO-	MSEN0	MTR0-	INDEX-	WDATA-	GND (Shield)
11	DR1-	DSKCHG-	MTR1-	DENSL	RDATA-	GND (Shield)
10	WP-	HDSEL-	DIR-	TRK0-	STEP-	GND (Shield)
9	WGATE-	ERR-	AFD-	BUSY	USB+	GND (Shield)
8	PE	SLIN-	VCC	STB-	USB-	GND (Shield)
7	PPD7	PPD6	PPD5	PPD4	INIT-	GND (Shield)
6	PPD3	PPD2	PPD1	PPD0	ACK-	GND (Shield)
5	ABORT-	MSDAT	SPKR	KBDAT	SLCT	GND (Shield)
4	PRST	MSCLK	VCC	KBCLK	S1RXD	GND (Shield)
3	S1CTS	S1RTS	S1DSR	S1DCD	S1TXD	GND (Shield)
2	S2RIN	S2DTR	S1RIN	S1DTR	S2RXD	GND (Shield)
1	S2CTS	S2RTS	S2DSR	S2DCD	S2TXD	GND (Shield)
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

J6 (Universal Serial Bus (USB) Port Interface Connector)

J6 is the Universal Serial Bus (USB) Interface. See the "J6 Universal Serial Bus (USB) Port Interface Connector Pinout" table below for pin definitions.

J6 Universal Serial Bus (USB) Port Interface Connector Pinout

Pin #	Function
1	Vcc (Fused)
2	DATA-
3	DATA+
4	GND

J7, J8 (Video Output/Video Input Connectors)

J7 (male, output) and J8 (female, input) are 16-pin 2 mm connectors which pass straight through to each other and allow a zPM 10/11 Video Module to be used on the ZT 5520. See the "J7, J8 Video Output/Video Input Connectors Pinout" table below for pin definitions.

J7, J8 Video Output/Video Input Connector Pinout

J7	Function	J8
pin 1	connects to	pin 1
pin 2	connects to	pin 2
pin 3	connects to	pin 3
pin 4	connects to	pin 4
pin 5	connects to	pin 5
pin 6	connects to	pin 6
pin 7	connects to	pin 7
pin 8	connects to	pin 8
pin 9	connects to	pin 9
pin 10	connects to	pin 10
pin 11	connects to	pin 11
pin 12	connects to	pin 12
pin 13	connects to	pin 13
pin 14	connects to	pin 14
pin 15	connects to	pin 15
pin 16	connects to	pin 16

J9 (Keyboard Interface Connector)

J9 allows interfacing to standard PS/2 style keyboard devices. See the "J9 Keyboard Interface Connector Pinout" table below for pin definitions.

J9 Keyboard Interface Connector Pinout

Pin#	Function
1	KBDAT
2	No Connect
3	GND
4	Vcc (Fused)
5	KBCLK
6	No Connect

J10 (Reserved)

Connector J10 is reserved for Ziatech use.

J11, J16, J20 (Fan Power Connectors)

J11 provides power for the front panel Voltage Regulator Module (VRM) cooling fan. J16 and J20 provide power for the CPU fan/heatsinks (J16 = CPU2; J20 = CPU1). Select +12 VDC or +5 VDC configuration with cuttable traces CT1 and CT30.

See the "J11, J16, J20 Fan Power Connector Pinout" table below for pin definitions.

J11, J16, J20 Fan Power Connector Pinout

Pin#	Function
1	Fan Power (+12 VDC or +5 V, depending on the position of CT1 or CT30)
2	GND
3	Tachometer (optional for J11 only)

J12 (COM2 Connector), J13 (COM1 Connector)

J12 is COM2 and J13 is COM1. See the "J12 (COM2 Connector), J13 (COM1 Connector) Pinout" table below for pin definitions.

J12 COM2 Connector, J13 COM1 Connector Pinout

Pin#	Function
1	DCD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RIN

J14 (PLD Programming Interface Connector)

J14 is the In-System-Programming (ISP) port used during the manufacturing process to program on-board PLD devices. No user function exists. See the "J14 PLD Programming Interface Connector Pinout" table below for pin definitions.

J14 PLD Programming Interface Connector Pinout

Pin#	Function
1	GND
2	SDO (Data from ISP chain)
3	GND
4	SCK (Clock)
5	GND
6	SMS (Mode)
7	GND
8	SDI (Data to ISP chain)
9	Vcc
10	SRST- (Reset)

J15 (General JTAG Interface Connector)

J15 allows ICT equipment to access the TAP function for all on-board JTAG devices (except the Pentium Pro processors, which are accessed through connector J21). This interface must be driven by TTL technology to operate correctly. See the "J15 General JTAG Interface Connector Pinout" table below for pin definitions.

J15 General JTAG Interface Connector Pinout

Pin#	Function
1	GND
2	TDO (Data from device)
3	GND
4	TCK (Clock)
5	GND
6	TMS (Mode)
7	GND
8	TDI (Data to device)
9	Vcc
10	TRST- (Reset)

J17 (Flash/IDE Expansion Connector)

J17 provides the signals for optional on-board solid state IDE expansion via the ZT 96061 CompactFlash™-to-IDE Mezzanine Adapter. Eight bits of DI/O are also available on this connector. This connector is implemented with a 100-pin female 0.050" x 0.050" micro pitch terminal. See the "J17 Flash/IDE Expansion Connector Pinout" table below for pin definitions. See the section "Solid State IDE Option" in Chapter 17, "Enhanced IDE Interface," for more information on the CompactFlash option.

J17 Flash/IDE Expansion Connector Pinout

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
A1	Vcc	B1	Vcc	A26	FLCE2	B26	DD10
A2	GND	B2	GND	A27	FLCE1	B27	DD9
A3	SA0	B3	XD0	A28	FLWP	B28	DD8
A4	SA1	B4	XD1	A29	PWRGD	B29	DD7
A5	SA2	B5	XD2	A30	IOR-	B30	DD6
A6	SA3	B6	XD3	A31	IOW-	B31	DD5
A7	SA4	B7	XD4	A32	PCS-	B32	DD4
A8	SA5	B8	XD5	A33	SCLK	B33	DD3
A9	SA6	B9	XD6	A34	IDEACK	B34	DD2
A10	SA7	B10	XD7	A35	SC	B35	DD1
A11	SA8	B11	EXCE0	A36	SC	B36	DD0
A12	SA9	B12	EXCE1	A37	SC	B37	IO16-
A13	SA10	B13	EXCE2	A38	SC	B38	CS3P-
A14	SA11	B14	EXCE3	A39	DIGIO0	B39	CS1P-
A15	SA12	B15	EXCE4	A40	DIGIO1	B40	DA2
A16	SA12	B16	EXCE5	A41	DIGIO2	B41	DA1
A17	SA14	B17	EXCE6	A42	DIGIO3	B42	DA0
A18	SA15	B18	EXCE7	A43	DIGIO4	B43	IRQ14
A19	SA16	B19	VCCS	A44	DIGIO5	B44	DDAK0-
A20	PGA17	B20	SCEB-	A45	DIGIO6	B45	IORDY
A21	PGA18	B21	DD15	A46	DIGIO7	B46	DIOR-
A22	PGA19	B22	DD14	A47	12V	B47	DIOW-
A23	PGA20	B23	DD13	A48	GND	B48	DDRQ0
A24	MEMR-	B24	DD12	A49	Vcc	B49	Vcc
A25	MEMW-	B25	DD11	A50	GND	B50	GND

J18 (Mezzanine PCI Interface Connector)

J18 provides PCI signals for a CompactPCI mezzanine interface. See the "J18 Mezzanine PCI Interface Connector Pinout" table below for pin definitions.

J18 Mezzanine PCI Interface Connector Pinout

Pin#	A	B	C	D	E	F
25	5V	REQ64#	NC	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	SDONE	SBO#	GND	PERR#	GND
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	3.3V	CLK	AD[31]	GND
5	NC	NC	RST#	GND	GNT#	GND
4	NC	GND	V(I/O)	NC	NC	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

J19 (DRAM Interface Connector)

J19 provides connection for ECC, Parity or Non-Parity DRAM modules. Specialized memory modules are used for this interface. Up to four memory modules may be stacked at J19. No pinout information is available for this connector. Contact Ziatech for additional information.

J21 (Pentium Pro ITP Interface Connector)

J21 allows ITP (In Target Probe) equipment to access the TAP function exclusively for the Pentium Pro processor. This interface must be driven by 3.3 V technology for correct operation. TAP function access for all other on-board JTAG devices is provided through connector J15. See the "J21 Pentium Pro ITP Interface Connector Pinout" table below for pin definitions.

J21 Pentium Pro ITP Interface Connector Pinout

Pin#	Function	Pin#	Function
1	RESET#	16	PREQ0#
2	GND	17	GND
3	DBRESET#	18	PRDY0#
4	GND	19	GND
5	TCK	20	PREQ1#
6	GND	21	GND
7	TMS	22	PRDY1#
8	TDI	23	GND
9	POWERON	24	PREQ2#
10	TDO	25	GND
11	DBINST#	26	PRDY2#
12	TRST#	27	GND
13	GND	28	PREQ3#
14	BSEN#	29	GND
15	GND	30	PRDY3#

J22 (Floppy Disk Drive Interface Connector)

J22 is implemented as a 26-pin 1 mm standard interface (located on the solder-side of the board) for a 3.5" floppy disk. See the "J22 Floppy Disk Drive Interface Connector Pinout" table below for pin definitions.

J22 Floppy Disk Drive Interface Connector Pinout

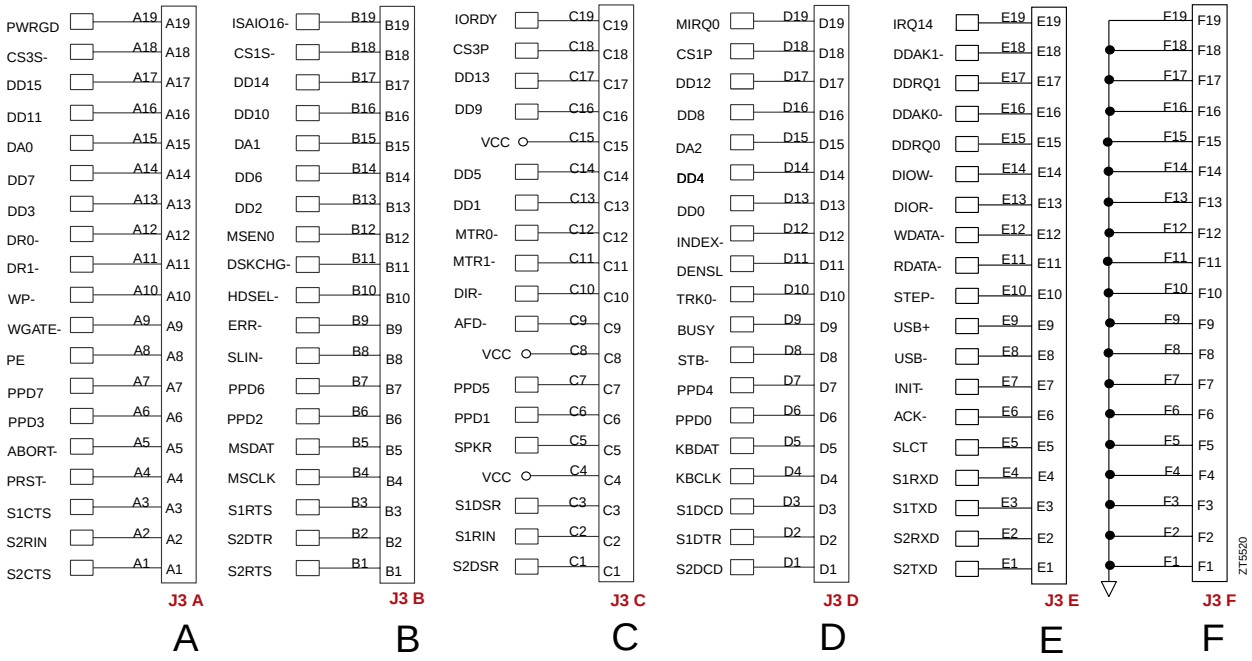
Pin#	Function	Pin#	Function
1	Vcc	2	INDEX
3	Vcc	4	DRSEL0
5	Vcc	6	DSKCHG
7	DRSEL1	8	READY
9	DENSTAT	10	MOTON
11	DENSEL	12	DIR
13	GND	14	STEP
15	GND	16	WDATA
17	GND	18	WGATE
19	GND	20	TRK0
21	GND	22	WP
23	GND	24	RDATA
25	GND	26	HDSEL

SCHEMATICS: REAR-PANEL USER I/O CONNECTION

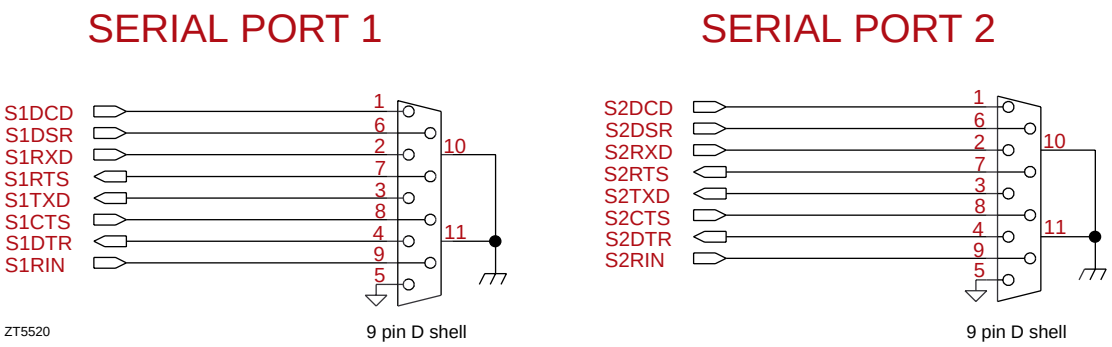
The list below provides links to example schematics showing standard connection of various peripherals to the "J3 Rear-Panel User I/O Connector".

- Backplane I/O Connection Example Schematic
- Serial Ports 1 and 2 Connection Example Schematics
- Status Port Connection Example Schematic
- Universal Serial Bus (USB) Connection Example Schematic
- Printer Port Connection Example Schematic
- Keyboard and Mouse Connection Example Schematic

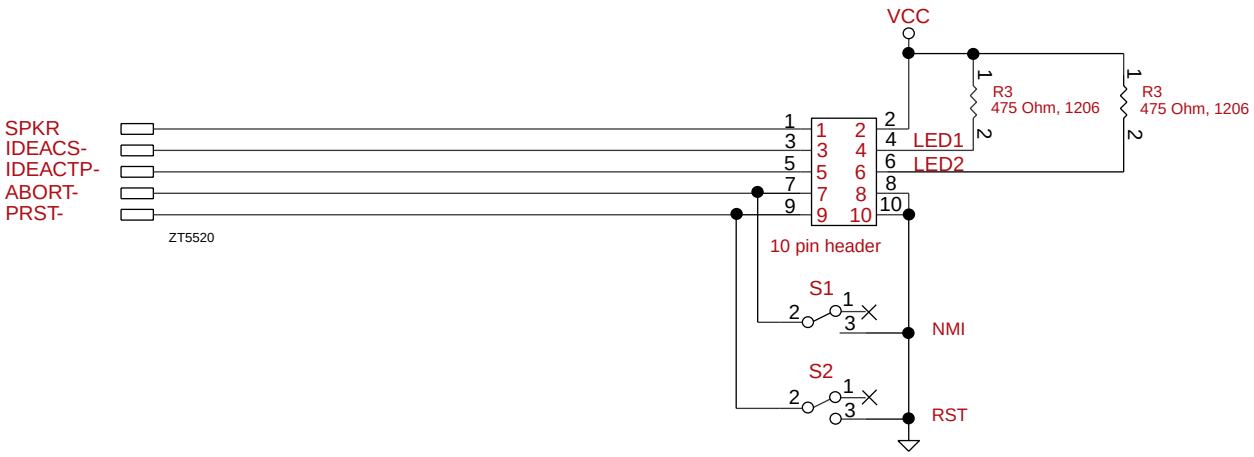
- Floppy Connection Example Schematic
- IDE (Primary and Secondary) Connection Example Schematic



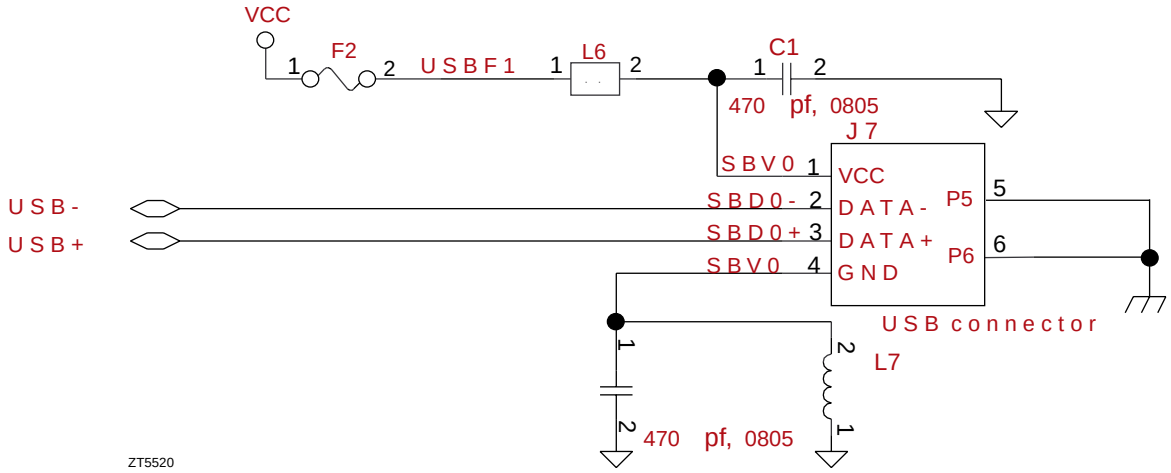
Backplane I/O Connection Example Schematic



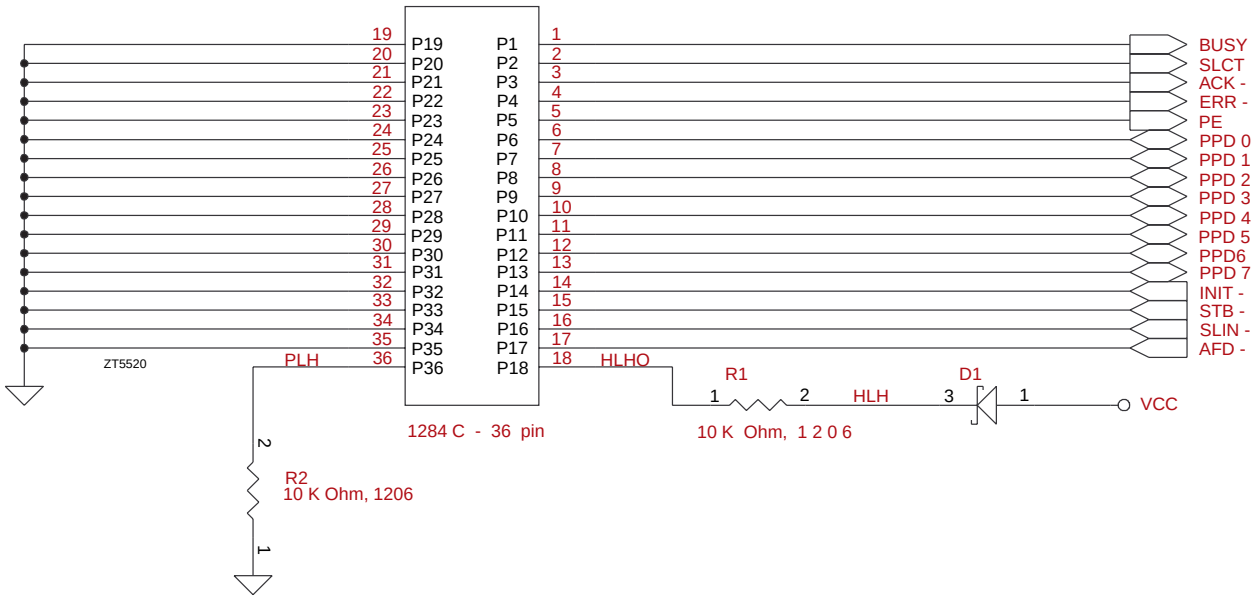
Serial Ports 1 and 2 Connection Example Schematics



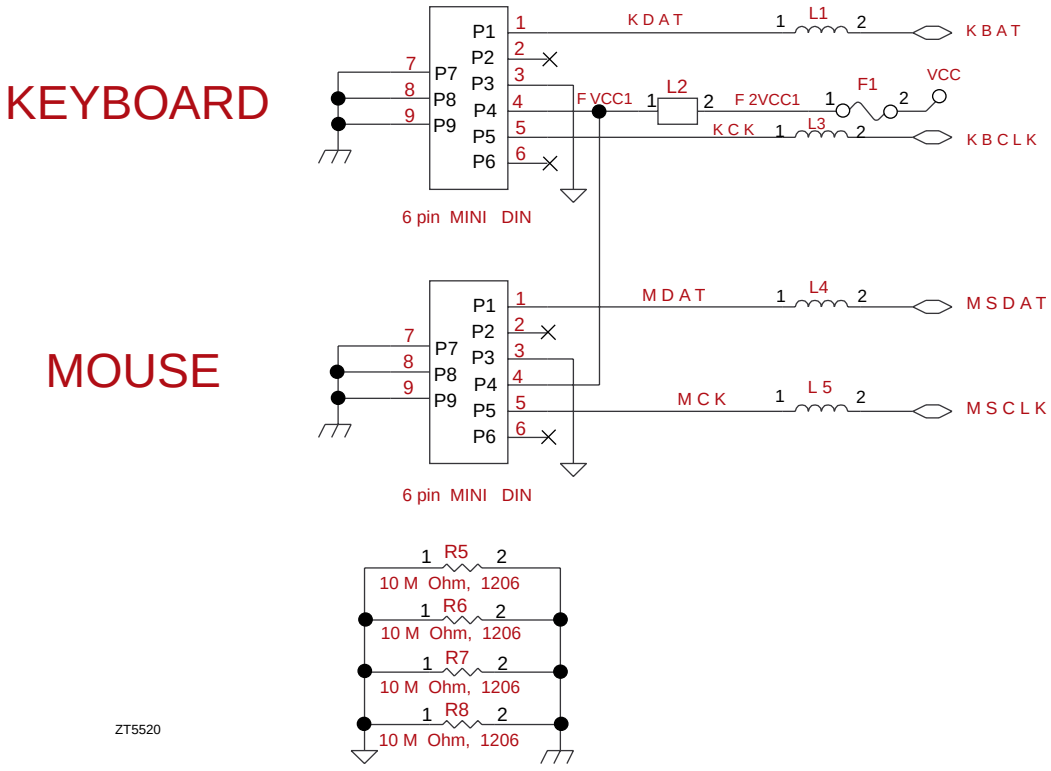
Status Port Connection Example Schematic



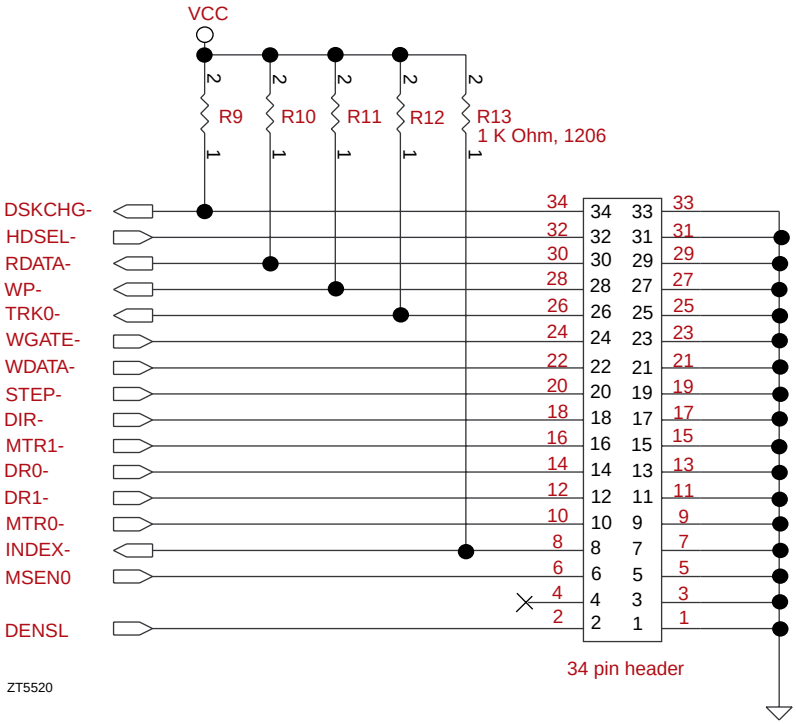
Universal Serial Bus (USB) Connection Example Schematic



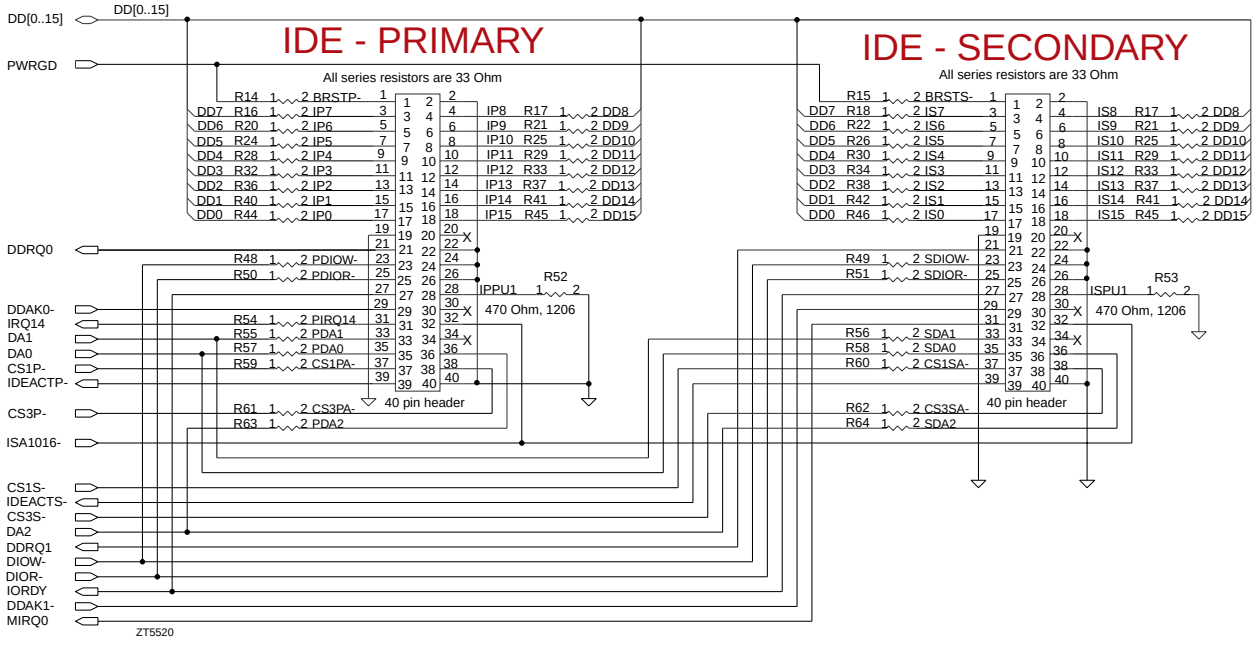
Printer Port Connection Example Schematic



Keyboard and Mouse Connection Example Schematics



Floppy Connection Example Schematic



IDE (Primary and Secondary) Connection Example Schematic

C. DIGITAL I/O ASIC SYSTEM SETUP CONSIDERATIONS

The purpose of this appendix is to illustrate precautions you should take to prevent latchup conditions and protect inputs.

The 16C50A Digital I/O ASIC device used on the ZT 5520 is designed by Ziatech to offer bi-directional I/O signals with or without event sense capability. This device features low power, high speed, wide temperature operation achievable only by utilizing CMOS technology.

Although CMOS technology offers many advantages, you must observe a few cautions when interfacing to any CMOS parts.

CMOS inputs and outputs can exhibit latchup characteristics. These inherent characteristics of any CMOS technology can result in the formation of a Silicon-Controlled Rectifier (SCR) that appears between Vcc and ground when voltages greater than Vcc or less than ground are applied to inputs or outputs. When this happens, Vcc is effectively shorted to ground. The only way to remove the latchup condition is to shut off the power supply. If a large current is allowed to flow through the chip, its operating temperature may increase, it may exhibit intermittent operation, or it may be damaged.

CMOS inputs must be protected from slow rising signals and inductive coupling on their inputs. Failure to do so will allow a potentially large current to flow through the chip, damaging the chip.

For more information on how the Digital I/O ASIC works, see the section "Functional Description" in Chapter 13, "Parallel I/O".

Several ports of the on-board 16C50A Digital I/O ASIC device are used for monitoring and controlling other board functions. See the section, "Digital I/O ASIC Definitions," in Chapter 11 for more information.

PREVENTING SYSTEM LATCHUP

The most common causes of latchup are:

- Input signals applied before the input circuitry is powered, resulting in a signal to power supply sequence mismatch
- Input signals greater than Vcc or less than ground, resulting in a signal level mismatch

Each of these conditions is covered in the following topics.

Power Supply Sequence Mismatch

A common application is to interface to a 24-position ZT 2226, Opto 22, or equivalent I/O module rack. Vcc and ground are provided from the ZT 5520 through connector J17 with Vcc protected by a 1 A fuse. This application is illustrated in Figure 1. In this application, no power supply sequence mismatch exists because the power supplying the input circuitry within the Digital I/O ASIC is applied before or at the same time as the power supplying the external signals. Proper system operation will result.

However, if a power source other than that supplying the Digital I/O ASIC is used to power the external signals, then a power sequence mismatch could occur, resulting in a latchup condition. An external power source might be required if the external circuitry requires more than the 1 A supplied by the cable or if a custom interface is being designed (see Figure 2 for an example).

One solution is to switch the external signals' power supply with an output that is controlled by the computer. In this manner, if the computer is off, so is the external power supply. This solution is illustrated in Figure 3.

A simpler solution is to power the relay controlling the external power supply directly from Vcc and ground supplied by the interface cable.

Another solution is to utilize the same switch to control the computer's power supply and the external signals' power supply, as illustrated in Figure 4. This is an acceptable solution for power supply sequence mismatches as long as the computer supply ramps up faster than the external power supply. This ensures the Digital I/O ASIC input circuitry is powered before the external signal circuitry.

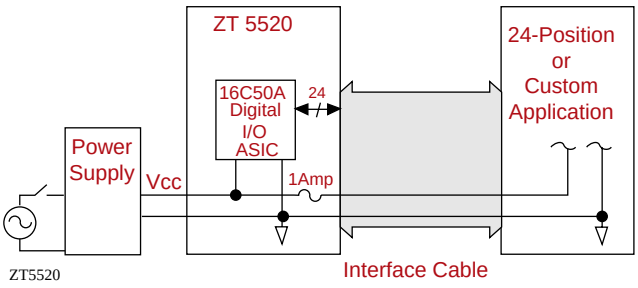


Figure 1. I/O Rack Vcc and Ground Supplied Via Interface Cable

Correct Power Supply Sequence, Signal Level Matched

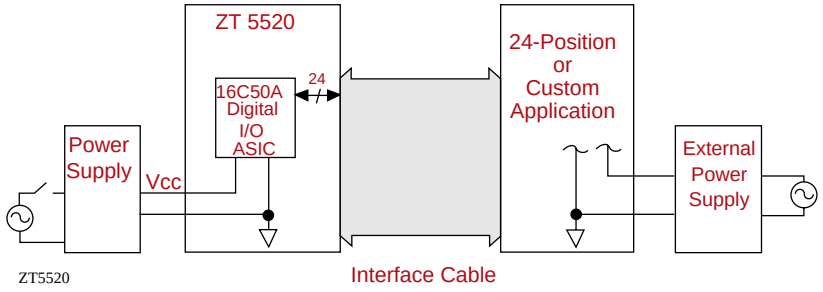


Figure 2. I/O Rack Vcc and Ground Supplied Externally

Potential Power Supply Sequence Mismatch, Signal Level Mismatch

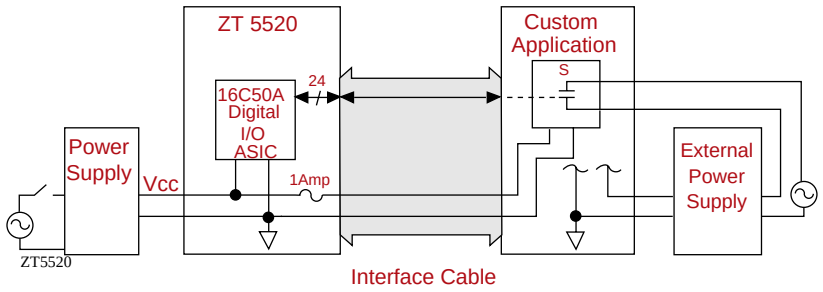


Figure 3. Computer-Switched External Power Supply

Correct Power Supply Sequence, Potential Signal Level Mismatch

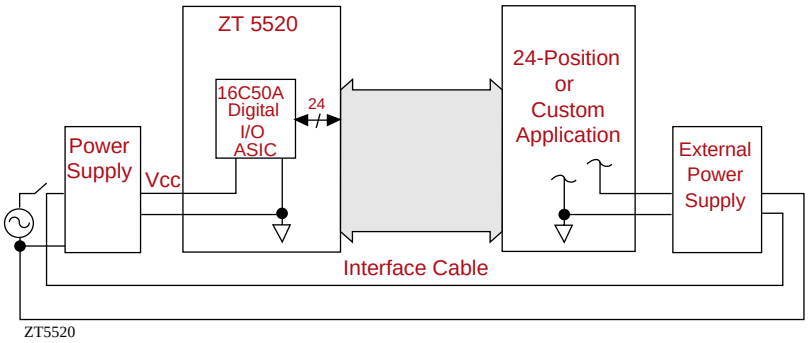


Figure 4. Computer and External Power Supply with Common Switch

Correct Power Supply Sequence, Potential Signal Level Mismatch

Signal Level Mismatch

Power supplying the external signal in Figure 1 is always relative to the Digital I/O ASIC input circuitry power because power is provided over the interface cable. Signal level mismatches will not occur and proper system operation will result. However, if separate power supplies are used, there are two predominant causes of signal level mismatches.

The first (assuming no sequencing problems) occurs when the two supplies are not referenced to each other, as illustrated in Figures 2, 3, and 4, This results in signals that may be higher than Vcc or lower than ground, potentially causing SCR latchup. All that is generally needed is to reference one supply to the other, typically by connecting a common ground. The most convenient way of connecting a common ground is to use the interface cable. Figures 5, 6, and 7 illustrate correct ground connections.

The second cause of mismatch occurs when the two power supplies are referenced to each other but the Vcc difference between the two power supplies exceeds 0.5 V. This results in signals that could be greater than Vcc, causing SCR latchup. This is easily remedied by adjusting the external power supply voltage to be within 0.5 V of the computer power supply voltage.

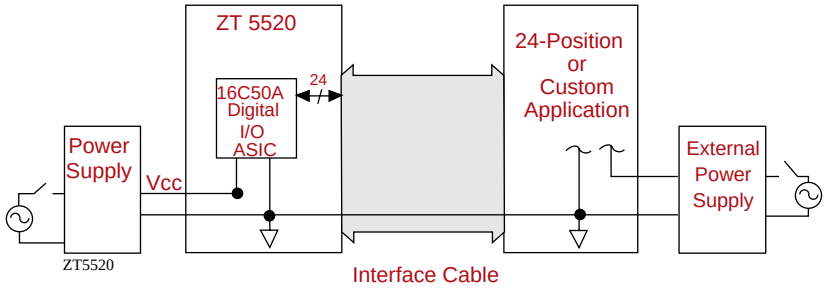


Figure 5. I/O Rack Vcc Supplied Externally, Common Ground

Potential Power Supply Seq. Mismatch, Correct Signal Level Match

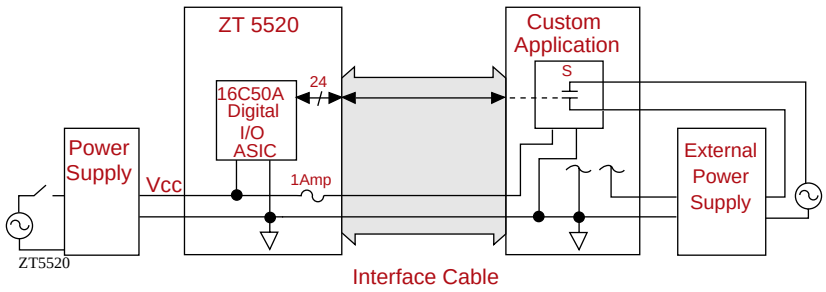


Figure 6. Computer-Switched External Power Supply, Common Ground

Correct Power Supply Sequence, Correct Signal Level Match

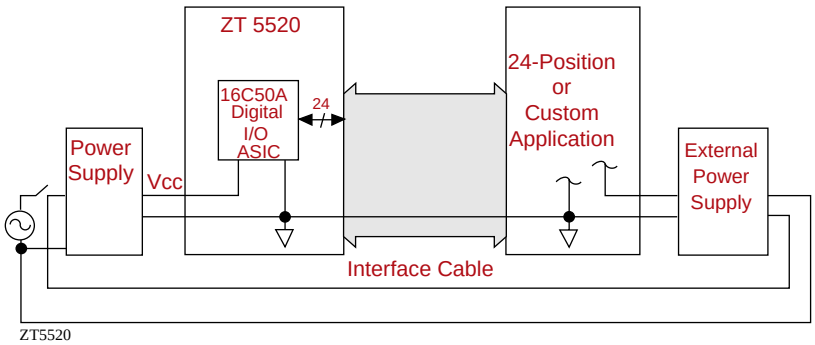


Figure 7. Computer and External Power Supply with Common Switch and Ground

Correct Power Supply Sequence, Correct Signal Level Match

PROTECTING CMOS INPUTS

The most common causes of damaged inputs are:

- Slow rise times, resulting in a ground bounce within the chip
- Inductive coupling on I/O lines causing noise to be coupled into the chip, resulting in intermittent operation

Each of these conditions is covered in the following topics.

Rise Times

Slow rise times on a CMOS input can easily cause the transistor to bounce between Vil and Vih. When this oscillation occurs, the operating current goes up, resulting in "ground bounce." Ground bounce can cause internal latchup or can cause other system components to malfunction. A pullup termination resistor is used to increase the rise time.

Input rise times must be kept to less than 50 ns. Given a maximum chip capacitance of 10 pF, a 5k ohm resistor is the largest that could be used without additional cabling. As cabling is added, the capacitance goes up, resulting in the use of a smaller pullup resistor until the maximum sink current of the output is achieved.

If the 16C50A Digital I/O ASIC device is driving the output, its maximum sink current at a Vol of .4 V is 12 mA. This gives a lower limit of 420 ohms for the pullup resistor, allowing a maximum cabling capacitance of 110 pF. Note that while the input feature of the Digital I/O ASIC may not be used by your application (Digital I/O ASIC used as an output only), the input circuitry remains in parallel; therefore, the output rise time is still a critical parameter that the input still sees. The output rise time must not exceed 50 ns.

Be wary of using low pass filters to remove electrical noise. The resulting capacitance is typically too large to meet the 50 ns rise time requirement.

Typically, optical isolators are used to help remove electrical noise while providing for different grounds. Separate grounds are achieved through the use of an additional power supply for the optocoupler rather than using the computer's power supply. If the computer's power supply powers the optocouplers, electrical isolation is defeated. An example of one such circuit is illustrated in Figure 8. The circuit can be altered to allow for design considerations.

Assuming a Vil of 1 V maximum for the 16C50A Digital I/O ASIC, the HP Dual Optocoupler must have a Vol of less than or equal to 1 V over the operating temperature. Using a TTL-compatible optocoupler gives a Vol of .6 V maximum with rise and fall times (50 ns and 10 ns, respectively) that are easily compatible with the Digital I/O ASIC, given a 1k ohm pullup.

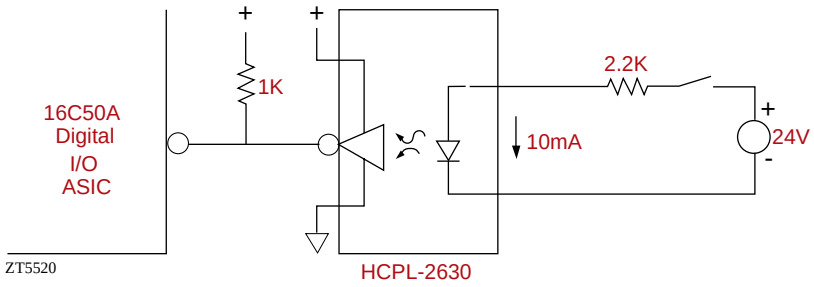


Figure 8. Digital I/O ASIC-to-Optocoupler Interface Example

Inductive Coupling

Inductive coupling on I/O lines can cause noise to be coupled into the chip, resulting in intermittent operation. This situation occurs when the Digital I/O ASIC I/O signals are routed with other signals within a wire bundle. One way to filter inductively coupled noise, or any noise for that matter, within a system with the same ground (not using optocouplers) is illustrated in Figure 9.

In the above circuit, the Texas Instruments 74S1053 Schottky diode clamps limit a transient to ±1 V above +5 V or below ground. The ferrite bead has a 50 ohm impedance at the frequency of interest. As the diodes begin to clamp and current flows through them, the voltage across the LCA05 5 V bidirectional TransZorbs® increases, causing them to conduct and allowing the majority of energy to flow through them instead of through the diode clamps.

The 39 pF capacitor, in conjunction with the ferrite bead, forms an additional low pass filter, and is entirely optional. The 1k ohm pullup ensures adequate rise time on the signal. The fuse acts as additional insurance against catastrophic events that might destroy the TransZorb and diode clamps.

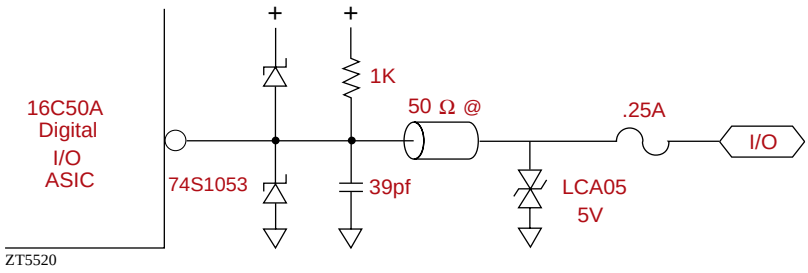


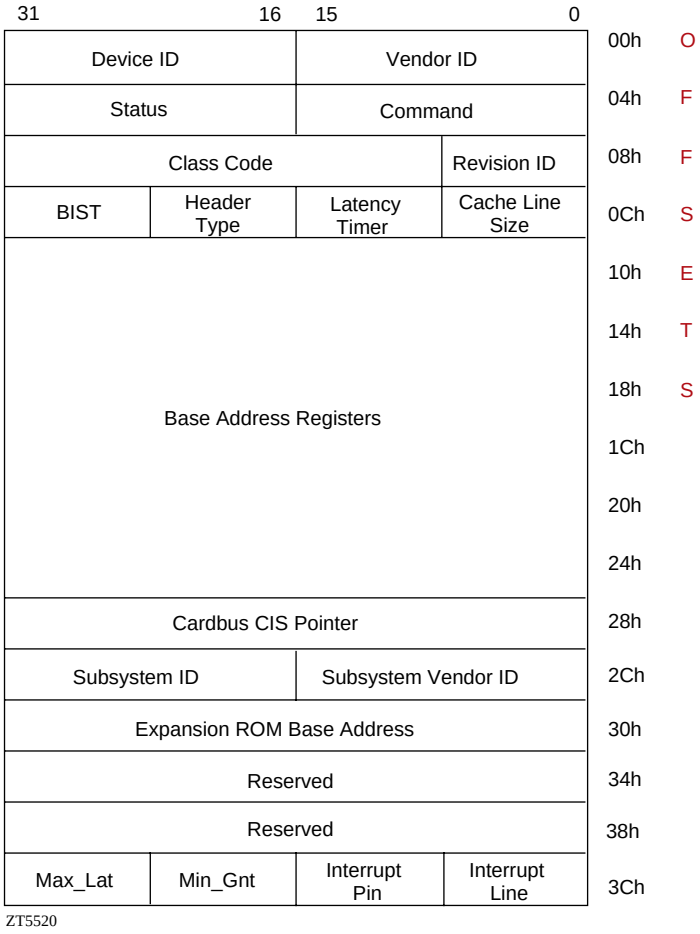
Figure 9. Digital I/O ASIC-to-Filter Interface Example

ADDITIONAL INFORMATION

You can find additional design information in the *Advanced CMOS Logic Designer's Handbook,* published by Texas Instruments.

D. PCI CONFIGURATION SPACE MAP

All PCI compliant devices contain a PCI configuration header. The generic layout of the header is shown in the "PCI Configuration Header" diagram below.



PCI Configuration Header

Additionally, a device may contain unique configuration registers (at location > 40h). For the ZT 5520, these are shown in the "On-Board Device PCI Bus Mapping" table. Details for each device's configuration space can be found in the respective manufacturer's data manuals. To obtain data manuals for the devices on the ZT 5520, refer to the list below.

Intel Corporation

Web: http://developer.intel.com

Phone: 800-628-8686

Digital Equipment Corporation

Web: http://www.digital.com

Phone: 800-332-2717

On-Board Device PCI Bus Mapping

Bus # (hex)	Dev # (hex)	Fcn # (hex)	Vendor ID	Device ID	Description
00	00	00	8086	1237	Intel 82441FX (PMC)
00	02	00	8086	7000	Intel 82371SB (PIIX3) PCI/ISA Bridge
00	02	01	8086	7010	Intel 82371SB (PIIX3) IDE Bus Master
00	02	02	8086	7020	Intel 82371SB (PIIX3) USB
00	04	00	†	†	Mezzanine Connector
00	08	00	1011	0025	DEC 21153 PCI Bridge
00	0C	00	1011	0025	DEC 21153 PCI Bridge

† The vendor and device ID will vary depending upon the device plugged into the mezzanine connector.

E. CUSTOMER SUPPORT

This appendix offers technical assistance information for this product, and also the necessary information should you need to return a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information are available at Ziatech's website, located at http://www.ziatech.com.

Corporate Headquarters

1050 Southwood Drive

San Luis Obispo, CA 93401 USA

Tel (805) 541-0488

FAX (805) 541-5088

RELIABILITY

Ziatech has taken extra care in the design of the product in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each product has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. The following information is needed to expedite the shipment of a replacement to you:

1. Your company name and address for invoice
2. Shipping address and phone number
3. Product I.D. number

4. If possible, the name of a technically qualified individual at your company familiar with the mode of failure on the board

If the unit is out of warranty, service is available at a predesignated service charge. Contact Ziatech for pricing and please supply a purchase order number for invoicing the repair.

Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it. ***Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!*** Mark the RMA number clearly on the outside of the box before returning.

ZIATECH WARRANTY

Ziatech provides a five-year limited warranty to its customers. Ziatech also has an explicit policy regarding the use of Ziatech products in life support systems. These topics are covered in the following sections.

Five-Year Limited Warranty

Products manufactured by Ziatech Corporation are covered from the date of purchase by a five-year warranty against defects in materials, workmanship, and published specifications applicable to the date of manufacture. During the warranty period, Ziatech will repair or replace, solely at its option, defective units provided they are returned at customer expense to an authorized Ziatech repair facility. Products which have been subjected to misuse, abuse, neglect, alteration, or unauthorized repair, determined at the sole discretion of Ziatech, whether by accident or otherwise, are excluded from warranty. The warranty on fans and disk drives is limited to two years and the warranty on flat panel displays is limited to nine months from date of purchase. Other products and accessories not manufactured by Ziatech are limited to the warranty provided by the original manufacturer. Consumable items (fuses, batteries, etc.) and software are not covered by this warranty.

Ziatech Corporation warrants that for a period of ninety (90) days from the date of purchase; the media on which software is furnished will be free of defects in materials and workmanship under normal use; and the software contains the features described in the Ziatech price list. Otherwise, the software is provided "AS IS". This limited warranty extends only to Customer as the original licensee. Customer's exclusive remedy and Ziatech's entire liability under this limited warranty will be, at Ziatech's option, to repair or replace the software, or refund the license fee paid therefore.

Ziatech may offer, where applicable and available, replacement products; otherwise, repairs requiring components, assemblies, and other purchased materials may be limited by market availability.

Ziatech assumes no liability resulting from changes to government regulations affecting use of materials, equipment, safety, and methods of repair. Ziatech may, at its discretion, offer replacement products.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY FOR FITNESS OF PURPOSE, MERCHANTABILITY, OR FREEDOM FROM INFRINGEMENT OR THE LIKE, AND ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATIONS, OR SAMPLE.

Ziatech neither assumes nor authorizes any person to assume for it any other liability. The liability of Ziatech under this warranty agreement is limited to a refund of the purchase price. In no event shall Ziatech be liable for loss of profits, use, incidental, consequential, or other damage, under this agreement.

Life Support Policy

Ziatech products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Ziatech Corporation. As used herein:

1. Life support devices or systems are devices or systems which support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, affect its safety, or limit its effectiveness.

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